

node of the signal output circuit 10 included in the gate driver 106 alternately changes between potentials of the VDD2 or VSS2.

[Patent Document 1] Japanese Patent Laid-Open No. 2004-126513 (FIGS. 12 and 13)

5 DISCLOSURE OF INVENTION

In general, a high potential power source and a low potential power source have a large potential difference. For example, if VDD1 is 10 V and VSS1 is 0V, there is a potential difference of 10 V between them. Meanwhile, if VDD2 is 12 V and VSS2 is - 2V, there is a potential difference of 14 V between them. When there is a large potential difference between
10 VDD1 and VSS1 and between VDD2 and VSS2, power consumption required for charging/discharging source lines and gate lines is increased.

In addition, in the case of using a time gray scale method for expressing gray scales, one frame is divided into multiple sub-frames, and source lines and gate lines are charged/discharged in each sub-frame period. That is, when the time gray scale method is used, the number of
15 charging/discharging operations of source lines and gate lines is increased, thereby power consumption is further increased.

Therefore, it is a primary object of the invention to provide a semiconductor device where power consumption required for charging/discharging source lines and gate lines can be reduced.

20 It is another object of the invention to provide a semiconductor device where power consumption can be reduced by controlling a potential difference between two signals outputted from an output node to be smaller than a potential difference between a high potential power source and a low potential power source.

A semiconductor device of the invention is supplied with potentials from a high
25 potential power source and a low potential power source. In addition, the semiconductor device of the invention has input and output nodes. Upon input of a signal to the input node, the output node outputs a signal having a first potential (also referred to as a first signal potential) and a signal having a second potential (also referred to as a second signal potential). According to the invention, a potential difference between the signal having a first potential and the signal
30 having a second potential is controlled to be smaller than a potential difference between the high

potential power source and the low potential power source, thereby power consumption is reduced.

A semiconductor device of the invention includes a first transistor, a second transistor and a third transistor connected in series, and a potential generating circuit. One of a source electrode and a drain electrode of the first transistor is connected to a high potential power source (also referred to as a first power source applying a first potential); a gate electrode of the third transistor is connected to the potential generating circuit; one of a source electrode and a drain electrode of the third transistor is connected to one of a source electrode and a drain electrode of the second transistor; and the other of the source electrode and the drain electrode of the third transistor is connected to a low potential power source (also referred to as a second power source applying a second potential). Upon input of a signal (first signal) to gate electrodes of the first transistor and the second transistor, a signal (second signal) is outputted from the other of the source electrode and the drain electrode of the first transistor and the other of the source electrode and the drain electrode of the second transistor.

In the aforementioned configuration, the first transistor is a p-channel transistor, the second transistor is an n-channel transistor, and the third transistor is a p-channel transistor.

A semiconductor device of the invention includes a first transistor, a second transistor and a third transistor connected in series, and a potential generating circuit. One of a source electrode and a drain electrode of the second transistor is connected to a low potential power source (also referred to as a second power source applying a second potential); a gate electrode of the third transistor is connected to the potential generating circuit; one of a source electrode and a drain electrode of the third transistor is connected to one of a source electrode and a drain electrode of the first transistor; and the other of the source electrode and the drain electrode of the third transistor is connected to a high potential power source (also referred to as a first power source applying a first potential). Upon input of a signal (first signal) to gate electrodes of the first transistor and the second transistor, a signal (second signal) is outputted from the other of the source electrode and the drain electrode of the first transistor and the other of the source electrode and the drain electrode of the second transistor.

In the aforementioned configuration, the first transistor is a p-channel transistor, the second transistor is an n-channel transistor, and the third transistor is an n-channel transistor.

A semiconductor device of the invention includes a first transistor, a second transistor, a third transistor and a fourth transistor connected in series, and potential generating circuits. Gate electrodes of the third transistor and the fourth transistor are connected to the potential generating circuits; one of a source electrode and a drain electrode of the third transistor is connected to one of a source electrode and a drain electrode of the second transistor; and the other of the source electrode and the drain electrode of the third transistor is connected to a low potential power source (also referred to as a second power source applying a second potential). One of a source electrode and a drain electrode of the fourth transistor is connected to one of a source electrode and a drain electrode of the first transistor; and the other of the source electrode and the drain electrode of the fourth transistor is connected to a high potential power source (also referred to as a first power source applying a first potential). Upon input of a signal (first signal) to gate electrodes of the first transistor and the second transistor, a signal (second signal) is outputted from the other of the source electrode and the drain electrode of the first transistor and the other of the source electrode and the drain electrode of the second transistor.

In the aforementioned configuration, the first transistor is a p-channel transistor, the second transistor is an n-channel transistor, the third transistor is a p-channel transistor, and the fourth transistor is an n-channel transistor.

A semiconductor device of the invention includes a first transistor and a second transistor connected in series, a third transistor and a fourth transistor connected in series, and a potential generating circuit. One of a source electrode and a drain electrode of the first transistor is connected to a high potential power source (also referred to as a first power source applying a first potential); one of a source electrode and a drain electrode of the second transistor is connected to a low potential power source (also referred to as a second power source applying a second potential); a gate electrode of the second transistor is connected to one of a source electrode and a drain electrode of the third transistor and to one of a source electrode and a drain electrode of the fourth transistor. The other of the source electrode and the drain electrode of the third transistor is connected to the high potential power source; and the other of the source electrode and the drain electrode of the fourth transistor is connected to the potential generating circuit. Upon input of a signal (first signal) to gate electrodes of the first transistor, the third transistor and the fourth transistor, a signal (second signal) is outputted from the other of the

DESCRIPTION

SEMICONDUCTOR DEVICE AND ELECTRONIC APPLIANCE USING THE SAME

5 TECHNICAL FIELD

The present invention relates to a semiconductor device which has input and output nodes, where a signal is outputted from the output node upon input of a signal to the input node. In addition, the invention relates to a semiconductor device including multiple transistors.

10 BACKGROUND ART

In recent years, semiconductor devices have been used in various electronic appliances, and development of the semiconductor devices are actively advanced. As one of the semiconductor devices, there is a semiconductor device having a source driver 101, a gate driver 106 and a pixel 110 (see FIG. 20A; and see Patent Document 1).

15 A signal output circuit 10 included in the source driver 101 is supplied with potentials from a high potential power source (VDD1) and a low potential power source (VSS1). The signal output circuit 10 included in the source driver 101 has input and output nodes, and the output node outputs a signal having the same potential as VDD1 or VSS1 upon input of a signal to the input node. The signal outputted from the signal output circuit 10 is inputted to a
20 p-channel transistor 113 through a source line 115 and an n-channel transistor 112, thereby the p-channel transistor 113 is turned on or off.

A signal output circuit 10 included in the gate driver 106 is supplied with potentials from a high potential power source (VDD2) and a low potential power source (VSS2). The signal output circuit 10 included in the gate driver 106 has input and output nodes, and the output
25 node outputs a signal having the same potential as VDD2 or VSS2 upon input of a signal to the input node. The signal outputted from the signal output circuit 10 is inputted to the n-channel transistor 112 through a gate line 116, thereby the n-channel transistor 112 is turned on or off.

A potential of the source line 115 connected to the output node of the signal output circuit 10 included in the source driver 101 alternately changes between potentials of the VDD1
30 and VSS1 (see FIG. 20B). Similarly, a potential of the gate line 116 connected to the output

source electrode and the drain electrode of the first transistor and the other of the source electrode and the drain electrode of the second transistor.

In the aforementioned configuration, the first transistor is a p-channel transistor, the second transistor is a p-channel transistor, the third transistor is a p-channel transistor, and the fourth transistor is an n-channel transistor.

A semiconductor device of the invention includes a first transistor and a second transistor connected in series, a third transistor and a fourth transistor connected in series, and a potential generating circuit. One of a source electrode and a drain electrode of the first transistor is connected to a high potential power source (also referred to as a first power source applying a first potential); one of a source electrode and a drain electrode of the second transistor is connected to a low potential power source (also referred to as a second power source applying a second potential); a gate electrode of the first transistor is connected to one of a source electrode and a drain electrode of the third transistor and to one of a source electrode and a drain electrode of the fourth transistor. The other of the source electrode and the drain electrode of the third transistor is connected to the low potential power source; and the other of the source electrode and the drain electrode of the fourth transistor is connected to the potential generating circuit. Upon input of a signal (first signal) to gate electrodes of the first transistor, the third transistor and the fourth transistor, a signal (second signal) is outputted from the other of the source electrode and the drain electrode of the first transistor and the other of the source electrode and the drain electrode of the second transistor.

In the aforementioned configuration, the first transistor is an n-channel transistor, the second transistor is an n-channel transistor, the third transistor is an n-channel transistor, and the fourth transistor is a p-channel transistor.

A semiconductor device of the invention includes a first transistor and a second transistor connected in series, a third transistor and a fourth transistor connected in series, a fifth transistor and a sixth transistor connected in series, and potential generating circuits. One of a source electrode and a drain electrode of the first transistor is connected to a high potential power source (also referred to as a first power source applying a first potential); and one of a source electrode and a drain electrode of the second transistor is connected to a low potential power source (also referred to as a second power source applying a second potential). A gate

electrode of the second transistor is connected to one of a source electrode and a drain electrode of the third transistor and to one of a source electrode and a drain electrode of the fourth transistor; the other of the source electrode and the drain electrode of the third transistor is connected to the high potential power source; and the other of the source electrode and the drain electrode of the fourth transistor is connected to the potential generating circuits. A gate electrode of the first transistor is connected to one of a source electrode and a drain electrode of the fifth transistor and to one of a source electrode and a drain electrode of the sixth transistor; the other of the source electrode and the drain electrode of the fifth transistor is connected to the low potential power source; and the other of the source electrode and the drain electrode of the sixth transistor is connected to the potential generating circuits. Upon input of a signal (first signal) to gate electrodes of the third to sixth transistors, a signal (second signal) is outputted from the other of the source electrode and the drain electrode of the first transistor and the other of the source electrode and the drain electrode of the second transistor.

In the aforementioned configuration, the first transistor is an n-channel transistor, the second transistor is a p-channel transistor, the third transistor is a p-channel transistor, the fourth transistor is an n-channel transistor, the fifth transistor is an n-channel transistor, and the sixth transistor is a p-channel transistor.

A semiconductor device of the invention includes a first transistor and a second transistor connected in series, and a subtraction circuit (also referred to as a circuit) including one or more subtraction transistors (also referred to as third transistors). One of a source electrode and a drain electrode of the first transistor is connected to a high potential power source (also referred to as a first power source applying a first potential); the subtraction circuit is provided between one of a source electrode and a drain electrode of the second transistor and a low potential power source (also referred to as a second power source applying a second potential); and a gate electrode of the subtraction transistor is connected to a drain electrode thereof. Upon input of a signal (first signal) to gate electrodes of the first and second transistors, a signal (second signal) is outputted from the other of the source electrode and the drain electrode of the first transistor and the other of the source electrode and the drain electrode of the second transistor.

In the aforementioned configuration, the first transistor is a p-channel transistor, the

second transistor is an n-channel transistor, and the subtraction transistor is an n-channel transistor.

In addition, in the aforementioned configuration, the multiple subtraction transistors included in the subtraction circuit are connected in series. One terminal of the subtraction
5 circuit is connected to the one of the source electrode and the drain electrode of the second transistor, and the other terminal of the subtraction circuit is kept at a potential of the low potential power source.

A semiconductor device of the invention includes a first transistor and a second transistor connected in series, and a subtraction circuit (also referred to as a circuit) including
10 one or more subtraction transistors (also referred to as third transistors). One of a source electrode and a drain electrode of the second transistor is connected to a low potential power source (also referred to as a second power source applying a second potential); the subtraction circuit is provided between one of a source electrode and a drain electrode of the first transistor and a high potential power source (also referred to as a first power source applying a first
15 potential); and a gate electrode of the subtraction transistor is connected to a drain electrode thereof. Upon input of a signal (first signal) to gate electrodes of the first transistor and the second transistor, a signal (second signal) is outputted from the other of the source electrode and the drain electrode of the first transistor and the other of the source electrode and the drain electrode of the second transistor.

20 In the aforementioned configuration, the first transistor is a p-channel transistor, the second transistor is an n-channel transistor, and the subtraction transistor is a p-channel transistor.

In addition, in the aforementioned configuration, one terminal of the subtraction circuit is connected to the one of the source electrode and the drain electrode of the first transistor, and
25 the other terminal of the subtraction circuit is kept at a potential of the high potential power source.

A semiconductor device of the invention includes a first transistor and a second transistor connected in series, a first subtraction circuit (also referred to as a first circuit) including one or more first subtraction transistors (also referred to as third transistors), and a
30 second subtraction circuit (also referred to as a second circuit) including one or more second

subtraction transistors (also referred to as fourth transistors). The first subtraction circuit is provided between one of a source electrode and a drain electrode of the second transistor and a low potential power source. The second subtraction circuit is provided between one of a source electrode and a drain electrode of the first transistor and a high potential power source. A gate electrode of the subtraction transistor is connected to a drain electrode thereof. Upon input of a signal (first signal) to gate electrodes of the first transistor and the second transistor, a signal (second signal) is outputted from the other of the source electrode and the drain electrode of the first transistor and the other of the source electrode and the drain electrode of the second transistor.

In the aforementioned configuration, the first transistor is a p-channel transistor, the second transistor is an n-channel transistor, the first subtraction transistor is an n-channel transistor, and the second subtraction transistor is a p-channel transistor.

In addition, in the aforementioned configuration, one terminal of the first subtraction circuit is connected to the one of the source electrode and the drain electrode of the first transistor, and the other terminal of the first subtraction circuit is kept at a potential of the low potential power source. Meanwhile, one terminal of the second subtraction circuit is connected to the one of the source electrode and the drain electrode of the second transistor, and the other terminal of the second subtraction circuit is kept at a potential of the high potential power source.

In all of the aforementioned configurations each including a subtraction circuit, if the subtraction circuit has one subtraction transistor, one terminal of the subtraction circuit corresponds to one of a source electrode and a drain electrode of the subtraction transistor. Meanwhile, the other terminal of the subtraction circuit corresponds to the other of the source electrode and the drain electrode of the subtraction transistor. On the other hand, if the subtraction circuit includes multiple subtraction transistors connected in series, one terminal of the subtraction circuit corresponds to one of a source electrode and a drain electrode of a subtraction transistor which is disposed at one end among the multiple subtraction transistors connected in series. Meanwhile, the other terminal of the subtraction circuit corresponds to one of a source electrode and a drain electrode of a subtraction transistor which is disposed at the other end among the multiple subtraction transistors connected in series.

The potential generating circuit included in the semiconductor device of the invention

has a first switch, a second switch, a first capacitor, a second capacitor, and a buffer amplifier. One node of the first switch is connected to a high potential power source for generating potentials; the other node of the first switch is connected to one node of the second switch and to one node of the first capacitor; the other node of the second switch is connected to one node of the second capacitor and to an input terminal of the buffer amplifier; and the other terminal of the second capacitor is connected to a low potential power source. Upon input of a subtraction signal (third signal) to the other node of the first capacitor, a fourth signal is outputted from an output node of the buffer amplifier. A potential of the fourth signal corresponds to a potential obtained by subtracting a potential of the subtraction signal from a potential of the high potential power source for generating potentials.

In the aforementioned configuration, the one node of the first switch which is connected to the high potential power source for generating potentials is kept at a potential of the high potential power source for generating potentials (also referred to as a fourth potential).

The potential generating circuit included in the semiconductor device of the invention has multiple resistors connected in series; one end of the multiple resistors is connected to a high potential power source while the other end thereof is connected to a low potential power source; and a potential is outputted from a connecting node of two resistors that are selected from among the multiple resistors.

In the semiconductor device having the aforementioned configuration, the node connected to the high potential power source and the node connected to the low potential power source are kept at constant potentials.

That is, the node connected to the high potential power source (also referred to as first power source) is kept at a potential of the high potential power source (also referred to as a first potential). Meanwhile, the node connected to the low potential power source (also referred to as a second power source) is kept at a potential of the low potential power source (also referred to as a second potential).

The potential generating circuit included in the semiconductor device of the invention generates a potential (also referred to as a third potential) which is different from potentials of the high potential power source and the low potential power source.

An electronic appliance of the invention has a semiconductor device of the invention

having any of the aforementioned configurations.

According to the invention having the aforementioned configurations, a potential difference between two signals outputted from an output node can be controlled to be smaller than a potential difference between the high potential power source and the low potential power source. As a result, the power consumption can be reduced.

BRIEF DESCRIPTION OF DRAWINGS

FIGS. 1A and 1B each illustrate a semiconductor device of the invention.

FIG. 2 illustrates a semiconductor device of the invention.

10 FIG. 3 illustrates a semiconductor device of the invention.

FIGS. 4A and 4B each illustrate a semiconductor device of the invention.

FIG. 5 illustrates a semiconductor device of the invention.

FIGS. 6A and 6B each illustrate a semiconductor device of the invention.

FIG. 7 illustrates a semiconductor device of the invention.

15 FIG. 8 illustrates a semiconductor device of the invention.

FIG. 9 illustrates a semiconductor device of the invention.

FIG. 10 illustrates a semiconductor device of the invention.

FIG. 11 illustrates a semiconductor device of the invention.

FIGS. 12A and 12B each illustrate a semiconductor device of the invention.

20 FIG. 13 illustrates a semiconductor device of the invention.

FIG. 14 illustrates a semiconductor device of the invention.

FIG. 15 illustrates a semiconductor device of the invention.

FIGS. 16A and 16B each illustrate a semiconductor device of the invention.

FIGS. 17A and 17B each illustrate a semiconductor device of the invention.

25 FIG. 18 illustrates an electronic appliance of the invention.

FIGS. 19A and 19F illustrate electronic appliances.

FIGS. 20A and 20B each illustrate a semiconductor device.

FIG. 21 illustrates a semiconductor device of the invention.

FIG. 22 illustrates a semiconductor device of the invention.

30 FIGS. 23A and 23B each illustrate a semiconductor device of the invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Although the invention will be fully described by way of embodiment modes and embodiments with reference to the accompanying drawings, it is to be understood that various changes and modifications will be apparent to those skilled in the art. Therefore, unless
5 otherwise such changes and modifications depart from the scope of the invention, they should be construed as being included therein. Note that in the constitution of the invention which is described below with reference to the drawings, identical portions are denoted by identical reference numerals in different drawings. In addition, in the description below, a high potential
10 power source and a low potential power source are denoted by VDD and VSS respectively in some cases. Further, an input node and an output node are denoted by In and OUT respectively in the drawings.

Embodiment Mode 1

15 Description is made with reference to the drawings on a configuration of the signal output circuit 10 which is a semiconductor device of the invention. The signal output circuit 10 outputs a signal from an output node (also called an output terminal) upon input of a signal to an input node (also called an input terminal).

The signal output circuit 10 of the invention includes transistors 11, 12 and 13
20 connected in series, and a potential generating circuit 14a (also referred to as a circuit 14a) (see FIG. 1A). The transistor 11 is a p-channel transistor, the transistor 12 is an n-channel transistor, and the transistor 13 is a p-channel transistor. The potential generating circuit 14a generates a potential V_a which is different from potentials of the high potential power source and the low potential power source, and the generated potential V_a is outputted to the transistor 13.

25 One of a source electrode and a drain electrode of the transistor 11 is connected to the high potential power source. A gate electrode of the transistor 13 is connected to the potential generating circuit 14a, and one of a source electrode and a drain electrode of the transistor 13 is connected to one of a source electrode and a drain electrode of the transistor 12 while the other
30 of the source electrode and the drain electrode of the transistor 13 is connected to the low potential power source.

The input node of the signal output circuit 10 corresponds to gate electrodes of the transistor 11 and the transistor 12. The output node of the signal output circuit 10 corresponds to the other of the source electrode and the drain electrode of the transistor 11 and to the other of the source electrode and the drain electrode of the transistor 12.

5 Description is made below on the operation of the signal output circuit 10 having the aforementioned configuration. In the description below, the high potential power source is 10 V, the low potential power source is 0 V, V_a is 4 V, and the threshold voltage of the transistor 13 is -1 V. In addition, a potential of an H-level signal is 10 V and a potential of an L-level signal is 0 V.

10 Upon input of an H-level signal to the input node of the signal output circuit 10, the transistor 11 is turned off while the transistor 12 is turned on. Since a potential of the gate electrode of the transistor 13 is V_a (here, 4 V), a potential of the drain electrode thereof is 0 V, and the threshold voltage thereof is -1 V, a potential of the source electrode of the transistor 13 is 5 V. Thus, the signal output circuit 10 outputs a signal of 5 V from the output node thereof.

15 Upon input of an L-level signal to the input node of the signal output circuit 10, the transistor 11 is turned on while the transistor 12 is turned off, and thus the output node of the signal output circuit 10 outputs a signal of 10 V which is the same level as the potential of VDD.

In the signal output circuit 10 having the aforementioned configuration, a potential difference between two signals outputted from the output node (5 V in the aforementioned example) can be smaller than the potential difference between the high potential power source and the low potential power source (10 V in the aforementioned example). As a result, the power consumption can be reduced.

20 The signal output circuit 10 of the invention includes transistors 11, 12 and 15 connected in series, and the potential generating circuit 14b (also referred to as a circuit 14b) (see FIG. 1B). The transistor 11 is a p-channel transistor, the transistor 12 is an n-channel transistor, and the transistor 15 is an n-channel transistor. The potential generating circuit 14b generates a potential V_b which is different from the potentials of the high potential power source and the low potential power source, and the generated potential V_b is outputted to the transistor 15.

30 One of the source electrode and the drain electrode of the transistor 12 is connected to the low potential power source. A gate electrode of the transistor 15 is connected to the

potential generating circuit 14b, and one of a source electrode and a drain electrode of the transistor 15 is connected to one of the source electrode and the drain electrode of the transistor 11 while the other of the source electrode and the drain electrode of the transistor 15 is connected to the high potential power source.

5 The input node of the signal output circuit 10 corresponds to the gate electrodes of the transistor 11 and the transistor 12. The output node of the signal output circuit 10 corresponds to the other of the source electrode and the drain electrode of the transistor 11 and to the other of the source electrode and the drain electrode of the transistor 12.

10 Description is made below on the operation of the signal output circuit 10 having the aforementioned configuration. In the description below, the high potential power source is 16 V, the low potential power source is 0 V, V_b is 10 V, and the threshold voltage of the transistor 15 is 1 V. In addition, a potential of an H-level signal is 16 V and a potential of an L-level signal is 0 V.

15 Upon input of an H-level signal to the input node of the signal output circuit 10, the transistor 11 is turned off while the transistor 12 is turned on, and the output node of the signal output circuit 10 outputs a signal of 0 V which is the same level as the potential of VSS.

20 Upon input of an L-level signal to the input node of the signal output circuit 10, the transistor 11 is turned on while the transistor 12 is turned off. Since a potential of the gate electrode of the transistor 15 is V_b (here, 10 V), a potential of the drain electrode thereof is 16 V, and the threshold voltage thereof 1 V, a potential of the source electrode of the transistor 15 is 9 V. Thus, the signal output circuit 10 outputs a signal of 9 V from the output node thereof.

25 In the signal output circuit 10 having the aforementioned configuration, a potential difference between two signals outputted from the output node (9 V in the aforementioned example) can be smaller than the potential difference between the high potential power source and the low potential power source (16 V in the aforementioned example). As a result, the power consumption can be reduced.

30 The signal output circuit 10 of the invention includes transistors 11, 12, 13 and 15 connected in series, the potential generating circuit 14a (also referred to as a first circuit 14a), and the potential generating circuit 14b (also referred to as a second circuit 14b)(see FIG. 2). The transistor 11 is a p-channel transistor, the transistor 12 is an n-channel transistor, the

transistor 13 is a p-channel transistor, and the transistor 15 is an n-channel transistor. The potential generating circuit 14a generates a potential Va which is different from the potentials of the high potential power source and the low potential power source, and the generated potential Va is outputted to the transistors 13. The potential generating circuit 14b generates a potential Vb which is different from the potentials of the high potential power source and the low potential power source, and the generated potential Vb is outputted to the transistors 15.

The aforementioned configuration of the signal output circuit 10 shown in FIG. 2 is obtained by combining the signal output circuit 10 shown in FIG. 1A and the signal output circuit 10 shown in FIG. 1B. Therefore, description on the operation of the aforementioned signal output circuit 10 shown in FIG. 2 is omitted.

Next, description is made on the case where multiple signal output circuits 10 are provided corresponding to multiple (x, where x is a natural number) wires (L1 to Lx) (see FIG. 3). Note that the multiple wires correspond to, for example, source lines or gate lines, and the multiple signal output circuits 10 are provided in a source driver or a gate driver. In the description below, the multiple signal output circuits 10 each having the configuration shown in FIG. 2 are provided.

In the case of providing the multiple signal output circuits 10, it is preferable to provide only an inverter 61 including the transistors 11 and 12 corresponding to each of the multiple wires (L1 to Lx). In addition, the multiple inverters 61 may share the transistors 13 and 15 and the potential generating circuit 14a and the potential generating circuit 14b. Accordingly, the number of elements can be reduced.

Note that in the aforementioned mode, the transistors 13 and 15 and the potential generating circuit 14a and the potential generating circuit 14b are provided corresponding to the multiple wires (L1 to Lx); however, the invention is not limited to this mode. For example, the multiple wires (L1 to Lx) may be divided into multiple groups, and the transistors 13 and 15 and the potential generating circuit 14a and the potential generating circuit 14b may be provided for each of the multiple groups.

In the aforementioned signal output circuits of the invention shown in FIGS. 1A to 3, a potential difference between two signals outputted from the output node can be controlled to be smaller than a potential difference between the high potential power source and the low potential

power source. As a result, the power consumption can be reduced. Note that there is a method of using a power source circuit having a high output current capability such as a series regulator or a charge pump in order to control a potential difference between two signals outputted from the output node to be smaller than a potential difference between the high potential power source and the low potential power source. However, this method cannot achieve sufficient power efficiency to reduce power consumption. Meanwhile, the aforementioned signal output circuits of the invention shown in FIGS. 1A to 3 cause only small power loss, and thus the power consumption can be reduced.

10 Embodiment Mode 2

The signal output circuit 10 which is a semiconductor device of the invention includes transistors 21 and 22 connected in series, transistors 23 and 24 connected in series, and the potential generating circuit 14a (also referred to as a circuit 14a) (see FIG. 4A). The transistor 21 is a p-channel transistor, the transistor 22 is a p-channel transistor, the transistor 23 is a p-channel transistor, and the transistor 24 is an n-channel transistor. The potential generating circuit 14a generates a potential V_a which is different from the potentials of the high potential power source and the low potential power source, and the generated potential V_a is outputted to the transistor 24.

One of a source electrode and a drain electrode of the transistor 21 is connected to the high potential power source. One of a source electrode and a drain electrode of the transistor 22 is connected to the low potential power source. A gate electrode of the transistor 22 is connected to one of a source electrode and a drain electrode of the transistor 23 and to one of a source electrode and a drain electrode of the transistor 24. The other of the source electrode and the drain electrode of the transistor 23 is connected to the high potential power source. The other of the source electrode and the drain electrode of the transistor 24 is connected to the potential generating circuit 14a.

An input node of the signal output circuit 10 correspond to gate electrodes of the transistors 21, 23 and 24. An output node of the signal output circuit 10 corresponds to the other of the source electrode and the drain electrode of the transistor 21 and to the other of the source electrode and the drain electrode of the transistor 22.

Description is made below on the operation of the signal output circuit 10 having the aforementioned configuration. In the description below, the high potential power source is 10 V, the low potential power source is 0 V, V_a is 4 V, and the threshold voltage of the transistor 22 is -1 V. In addition, a potential of an H-level signal is 10 V and a potential of an L-level signal is 0 V.

Upon input of an H-level signal to the input node of the signal output circuit 10, the transistors 21 and 23 are turned off while the transistor 24 is turned on. Then, the potential V_a (here, 4V) is supplied to the gate electrode of the transistor 22 through the transistor 24. Since a potential of the gate electrode of the transistor 22 is 4 V, a potential of the drain electrode thereof is 0 V, and the threshold voltage thereof is -1 V, a potential of the source electrode of the transistor 22 is 5 V. Thus, the signal output circuit 10 outputs a signal of 5 V from the output node thereof.

Upon input of an L-level signal to the input node of the signal output circuit 10, the transistors 21 and 23 are turned on while the transistor 24 is turned off. Then, the potential of the high potential power source is supplied to the gate electrode of the transistor 22 through the transistor 23, thereby the transistor 22 is turned off. Accordingly, the signal output circuit 10 outputs a signal of 10 V which is the same level as the potential of VDD from the output node thereof.

In the signal output circuit 10 having the aforementioned configuration, a potential difference between two signals outputted from the output node (5 V in the aforementioned example) can be smaller than the potential difference between the high potential power source and the low potential power source (10 V in the aforementioned example). As a result, the power consumption can be reduced.

The signal output circuit 10 of the invention includes the transistors 21 and 22 connected in series, transistors 25 and 26 connected in series, and the potential generating circuit 14b (also referred to as a circuit 14b) (see FIG. 4B). The transistor 21 is an n-channel transistor, the transistor 22 is an n-channel transistor, the transistor 25 is an n-channel transistor, and the transistor 26 is a p-channel transistor. The potential generating circuit 14b generates a potential V_b which is different from the potentials of the high potential power source and the low potential power source, and the generated potential V_b is outputted to the transistor 26.

One of the source electrode and the drain electrode of the transistor 21 is connected to the high potential power source. One of the source electrode and the drain electrode of the transistor 22 is connected to the low potential power source. The gate electrode of the transistor 21 is connected to one of a source electrode and a drain electrode of the transistor 25 and to one of a source electrode and a drain electrode of the transistor 26. The other of the source electrode and the drain electrode of the transistor 25 is connected to the low potential power source. The other of the source electrode and the drain electrode of the transistor 26 is connected to the potential generating circuit 14b.

An input node of the signal output circuit 10 correspond to gate electrodes of the transistors 22, 25 and 26. An output node of the signal output circuit 10 corresponds to the other of the source electrode and the drain electrode of the transistor 21 and to the other of the source electrode and the drain electrode of the transistor 22.

Description is made below on the operation of the signal output circuit 10 having the aforementioned configuration. In the description below, the high potential power source is 16 V, the low potential power source is 0 V, V_b is 10 V, and the threshold voltage of the transistor 21 is 1 V. In addition, a potential of an H-level signal is 16 V and a potential of an L-level signal is 0 V.

Upon input of an H-level signal to the input node of the signal output circuit 10, the transistors 22 and 25 are turned on while the transistor 26 is turned off. Then, a potential of the low potential power source is supplied to the gate electrode of the transistor 21 through the transistor 25, thereby the transistor 21 is turned off. Thus, the signal output circuit 10 outputs a signal of 0 V which is the same level as the potential of the VSS from the output node thereof.

Upon input of an L-level signal to the input node of the signal output circuit 10, the transistors 22 and 25 are turned off while the transistor 25 is turned on. Then, the potential V_b (here, 10 V) is supplied to the gate electrode of the transistor 21 through the transistor 26. Since a potential of the gate electrode of the transistor 21 is 10 V, a potential of the drain electrode thereof is 16 V, and the threshold voltage thereof is 1 V, a potential of the source electrode of the transistor 21 is 9 V. Accordingly, the signal output circuit 10 outputs a signal of 9 V from the output node thereof.

In the signal output circuit 10 having the aforementioned configuration, a potential

difference between two signals outputted from the output node (9 V in the aforementioned example) can be smaller than the potential difference between the high potential power source and the low potential power source (16 V in the aforementioned example). As a result, the power consumption can be reduced.

5 The signal output circuit 10 of the invention includes the transistors 21 and 22 connected in series, the transistors 23 and 24 connected in series, the transistors 25 and 26 connected in series, and the potential generating circuits 14a (also referred to as a first circuit 14a) and the potential generating circuit 14b (also referred to as a second circuit 14b) (see FIG. 5). The transistor 21 is an n-channel transistor, the transistor 22 is a p-channel transistor, the
10 transistor 23 is a p-channel transistor, the transistor 24 is an n-channel transistor, the transistor 25 is an n-channel transistor, and the transistor 26 is a p-channel transistor. The potential generating circuit 14a generates a potential V_a which is different from the potentials of the high potential power source and the low potential power source, and the generated potential V_a is outputted to the transistor 24. The potential generating circuit 14b generates a potential V_b
15 which is different from the potentials of the high potential power source and the low potential power source, and the generated potential V_b is outputted to the transistor 26.

One of the source electrode and the drain electrode of the transistor 21 is connected to the high potential power source. One of the source electrode and the drain electrode of the transistor 22 is connected to the low potential power source. The gate electrode of the transistor
20 22 is connected to one of the source electrode and the drain electrode of the transistor 23 and to one of the source electrode and the drain electrode of the transistor 24. The other of the source electrode and the drain electrode of the transistor 23 is connected to the high potential power source. The other of the source electrode and the drain electrode of the transistor 24 is connected to the potential generating circuit 14a. The gate electrode of the transistor 21 is
25 connected to one of the source electrode and the drain electrode of the transistor 25 and to one of the source electrode and the drain electrode of the transistor 26. The other of the source electrode and the drain electrode of the transistor 25 is connected to the low potential power source. The other of the source electrode and the drain electrode of the transistor 26 is connected to the potential generating circuit 14b.

30 An input node of the signal output circuit 10 corresponds to the gate electrodes of the

transistors 23, 24, 25 and 26. An output node of the signal output circuit 10 corresponds to the other of the source electrode and the drain electrode of the transistor 21 and to the other of the source electrode and the drain electrode of the transistor 22.

Description is made below on the operation of the signal output circuit 10 having the
5 aforementioned configuration. In the description below, the high potential power source is 16 V, the low potential power source is 0 V, V_a is 2V, V_b is 10 V, the threshold voltage of the transistor 21 is 1 V, and the threshold voltage of the transistor 22 is -1 V.

Upon input of an H-level signal to the input node of the signal output circuit 10, the transistor 23 is turned off, the transistor 24 is turned on, the transistor 25 is turned on, and the
10 transistor 26 is turned off. Then, a potential of the low potential power source is supplied to the gate electrode of the transistor 21 through the transistor 25, thereby the transistor 21 is turned off. Meanwhile, the potential V_a (here, 2 V) is supplied to the gate electrode of the transistor 22 through the transistor 24. Since a potential of the gate electrode of the transistor 22 is 2 V, a potential of the drain electrode thereof is 0 V, and the threshold voltage thereof is -1 V, a
15 potential of the source electrode of the transistor 22 is 3 V. Accordingly, the signal output circuit 10 outputs a signal of 3 V from the output node thereof.

Upon input of an L-level signal to the input node of the signal output circuit 10, the transistor 23 is turned on, the transistor 24 is turned off, the transistor 25 is turned off, and the transistor 26 is turned on. Then, the potential of the high potential power source is supplied to
20 the gate electrode of the transistor 22 through the transistor 23, thereby the transistor 22 is turned off. Meanwhile, the potential V_b (here, 10 V) is supplied to the gate electrode of the transistor 21 through the transistor 26. Since a potential of the gate electrode of the transistor 21 is 10 V, a potential of the drain electrode thereof is 16 V, and the threshold voltage thereof is 1 V, a potential of the source electrode of the transistor 21 is 9 V. Accordingly, the signal output
25 circuit 10 outputs a signal of 9 V from the output node thereof.

In the signal output circuit 10 having the aforementioned configuration, a potential difference between two signals outputted from the output node (9 V in the aforementioned example) can be smaller than the potential difference between the high potential power source and the low potential power source (16 V in the aforementioned example). As a result, the
30 power consumption can be reduced.

Note that in the case of providing multiple signal output circuits 10 having the aforementioned configuration shown in FIG. 4A, 4B or 5, the potential generating circuit 14a and the potential generating circuit 14b are not required to be provided in each signal output circuit 10, but may be shared by the multiple signal output circuits 10. Accordingly, the number of elements can be reduced.

Note that there is a method of using a power source circuit having a high output current capability such as a series regulator or a charge pump in order to control a potential difference between two signals outputted from the output node to be smaller than a potential difference between the high potential power source and the low potential power source. However, this method cannot achieve sufficient power efficiency to reduce power consumption. Meanwhile, the aforementioned signal output circuits of the invention shown in FIGS. 4A to 5 cause only small power loss, and thus the power consumption can be reduced.

Embodiment Mode 3

The signal output circuit 10 which is a semiconductor device of the invention includes transistors 31 and 32 connected in series, and a subtraction circuit 35 including one or more subtraction transistors (see FIG. 6A). The transistor 31 is a p-channel transistor, the transistor 32 is an n-channel transistor, and the one or more subtraction transistors included in the subtraction circuit 35 is/are n-channel transistors. In the shown configuration, the subtraction circuit 35 includes two subtraction transistors 33 and 34 connected in series.

One of a source electrode and a drain electrode of the transistor 31 is connected to the high potential power source. The subtraction circuit 35 is provided between one of a source electrode and a drain electrode of the transistor 32 and the low potential power source. A gate electrode of the subtraction transistor 33 is connected to one of a source electrode and a drain electrode of the subtraction transistor 33. Similarly, a gate electrode of the subtraction transistor 34 is connected to one of a source electrode and a drain electrode of the subtraction transistor 34.

An input node of the signal output circuit 10 corresponds to gate electrodes of the transistor 31 and the transistor 32. An output node of the signal output circuit 10 corresponds to the other of the source electrode and the drain electrode of the transistor 31 and to the other of

the source electrode and the drain electrode of the transistor 32.

Description is made below on the operation of the signal output circuit 10 having the aforementioned configuration. In the description below, the high potential power source is 10 V, the low potential power source is 0 V, the threshold voltage of the transistor 33 is 2 V and the threshold voltage of the transistor 34 is 2 V. In addition, a potential of an H-level signal is 10 V and a potential of an L-level signal is 0 V.

Upon input of an H-level signal to the input node of the signal output circuit 10, the transistors 31 is turned off while the transistor 32 is turned on. Since a potential of the source electrode of the transistor 34 is 0 V and the threshold voltage thereof is 2 V, a potential of the drain electrode of the transistor 34 is 2 V. In addition, since a potential of the source electrode of the transistor 33 is 2 V and the threshold voltage thereof is 2 V, a potential of the drain electrode of the transistor 33 is 4 V. Thus, the signal output circuit 10 outputs a signal of 4 V from the output node thereof.

Upon input of an L-level signal to the input node of the signal output circuit 10, the transistor 31 is turned on while the transistor 32 is turned off, and the output node of the signal output circuit 10 outputs a signal of 10 V which is the same level as the potential of VDD.

In the signal output circuit 10 having the aforementioned configuration, a potential difference between two signals outputted from the output node (6 V in the aforementioned example) can be smaller than the potential difference between the high potential power source and the low potential power source (10 V in the aforementioned example). As a result, the power consumption can be reduced.

The signal output circuit 10 of the invention includes the transistors 31 and 32 connected in series, and a subtraction circuit 38 including one or more subtraction transistors (see FIG. 6B). The transistor 31 is a p-channel transistor, the transistor 32 is an n-channel transistor, and the one or more subtraction transistors included in the subtraction circuit 38 is/are p-channel transistors. In the shown configuration, the subtraction circuit 38 includes two subtraction transistors 36 and 37 connected in series.

One of the source electrode and the drain electrode of the transistor 32 is connected to the low potential power source. The subtraction circuit 38 is provided between one of the source electrode and the drain electrode of the transistor 31 and the high potential power source.

A gate electrode of the subtraction transistor 36 is connected to one of a source electrode and a drain electrode of the subtraction transistor 36. A gate electrode of the subtraction transistor 37 is connected to one of a source electrode and a drain electrode of the subtraction transistor 37.

5 An input node of the signal output circuit 10 corresponds to the gate electrodes of the transistor 31 and the transistor 32. An output node of the signal output circuit 10 corresponds to the other of the source electrode and the drain electrode of the transistor 31 and to the other of the source electrode and the drain electrode of the transistor 32.

Description is made below on the operation of the signal output circuit 10 having the aforementioned configuration. In the description below, the high potential power source is 10 V, the low potential power source is 0 V, the threshold voltage of the transistor 36 is -2 V and the threshold voltage of the transistor 37 is -2 V. In addition, a potential of an H-level signal is 10 V and a potential of an L-level signal is 0 V.

10 Upon input of an H-level signal to the input node of the signal output circuit 10, the transistor 31 is turned off while the transistor 32 is turned on, and the signal output circuit 10 outputs a signal of 0 V which is the same level as the potential of VSS.

15 Upon input of an L-level signal to the input node of the signal output circuit 10, the transistor 31 is turned on, and the transistor 32 is turned off. Since a potential of the source electrode of the transistor 36 is 10 V and the threshold voltage thereof is -2 V, a potential of the drain electrode of the transistor 36 is 8 V. In addition, since a potential of the source electrode of the transistor 37 is 8 V and the threshold voltage thereof is -2 V, a potential of the drain electrode of the transistor 37 is 6 V. Thus, the signal output circuit 10 outputs a signal of 6 V from the output node thereof.

20 In the signal output circuit 10 having the aforementioned configuration, a potential difference between two signals outputted from the output node (6 V in the aforementioned example) can be smaller than the potential difference between the high potential power source and the low potential power source (10 V in the aforementioned example). As a result, the power consumption can be reduced.

25 The signal output circuit 10 of the invention includes the transistors 31 and 32 connected in series, the subtraction circuit 35 including one or more subtraction transistors, and the subtraction circuit 38 including one or more subtraction transistors (see FIG. 7). In the

30

shown configuration, the subtraction circuit 35 includes the two subtraction transistors 33 and 34 connected in series while the subtraction circuit 38 includes the two subtraction transistors 36 and 37 connected in series.

5 The subtraction circuit 35 is provided between one of the source electrode and the drain electrode of the transistor 32 and the low potential power source. Meanwhile, the subtraction circuit 38 is provided between one of the source electrode and the drain electrode of the transistor 31 and the high potential power source.

The aforementioned configuration of the signal output circuit 10 shown in FIG. 7 is obtained by combining the signal output circuit 10 shown in FIG. 6A and the signal output circuit 10 shown in FIG. 6B. Therefore, description on the operation of the aforementioned signal output circuit 10 shown in FIG. 7 is omitted.

Note that each of the aforementioned signal output circuits 10 shown in FIGS. 6A, 6B and 7 can be used as the potential generating circuit 14a and the potential generating circuit 14b.

15 Next, description is made on the case where the multiple signal output circuits 10 are provided corresponding to multiple (x , where x is a natural number) wires ($L1$ to Lx) (see FIG. 8). Note that the multiple wires correspond to, for example, source lines or gate lines, and the multiple signal output circuits 10 are provided in a source driver or a gate driver. In the description below, the multiple signal output circuits 10 having the configuration shown in FIG. 7 are provided.

20 In the case of providing the multiple signal output circuits 10, it is preferable to provide only the inverter 61 including the transistors 31 and 32 corresponding to each of the multiple wires ($L1$ to Lx). Then, the multiple inverters 61 may share the subtraction circuit 35 including the transistors 33 and 34 and the subtraction circuit 38 including the transistors 36 and 37. Accordingly, the number of elements can be reduced.

25 Note that in the aforementioned mode, the subtraction circuits 35 and 38 are provided corresponding to the multiple wires ($L1$ to Lx); however, the invention is not limited to this mode. For example, the multiple wires ($L1$ to Lx) may be divided into multiple groups, and the subtraction circuits 35 and 38 may be provided for each of the multiple groups.

30 In the aforementioned signal output circuits of the invention shown in FIGS. 6A to 8, a potential difference between two signals outputted from the output node can be controlled to be

smaller than a potential difference between the high potential power source and the low potential power source. As a result, the power consumption can be reduced. Note that there is a method of using a power source circuit having a high output current capability such as a series regulator or a charge pump in order to control a potential difference between two signals
5 outputted from the output node to be smaller than a potential difference between the high potential power source and the low potential power source. However, this method cannot achieve sufficient power efficiency to reduce power consumption. Meanwhile, the aforementioned signal output circuits of the invention shown in FIGS. 6A to 8 cause only small power loss, and thus the power consumption can be reduced.

10 In addition, the signal output circuits of the invention shown in FIGS. 6A to 8 have an advantage in that a potential generating circuit is not required as compared to the configurations shown in Embodiment Modes 1 and 2.

Embodiment Mode 4

15 A semiconductor device of the invention includes transistors 201 to 209 (see FIG. 9). The transistors 201, 203 to 205, 207 and 209 are p-channel transistors while the transistors 202, 206 and 208 are n-channel transistors.

Description is made on the operation of the semiconductor device having the aforementioned configuration. In the description below, the low potential power source is 0 V,
20 and all the transistors 203 to 205 and 209 have the same threshold voltage value ($|V_{THa}|$).

Upon input of an H-level signal to the input node, the transistor 201 is turned off, the transistor 202 is turned on, the transistor 207 is turned off, and the transistor 208 is turned on.

A drain electrode of the transistor 206 has a potential which is obtained by subtracting the threshold voltages of the transistors 203 to 205 from the high potential power source (VDD):
25 $(VDD - |V_{THa}| - |V_{THa}| - |V_{THa}|)$, and this potential is supplied to a gate electrode of the transistor 209. Since a drain electrode of the transistor 209 has the same potential as the low potential power source (0 V), a source electrode of the transistor 209 has a potential of $(VDD - |V_{THa}| - |V_{THa}|)$, and a signal having the potential of $(VDD - |V_{THa}| - |V_{THa}|)$ is outputted from the output node.

30 Upon input of an L-level signal to the input node, the transistor 201 is turned on, the

transistor 202 is turned off, the transistor 207 is turned on, and the transistor 208 is turned off, thereby a signal having the same potential as the high potential power source (VDD) is outputted from the output node.

The semiconductor device of the invention having a different configuration from the
5 aforementioned has transistors 210 to 218 (see FIG. 10). The transistors 210, 212 and 217 are p-channel transistors while the transistors 211, 213 to 216 and 218 are n-channel transistors.

Description is made on the operation of the semiconductor device having the aforementioned configuration. In the description below, all the transistors 213 to 215 and 216 have the same threshold voltage value ($|V_{THa}|$).

10 Upon input of an H-level signal to the input node, the transistor 201 is turned off, the transistor 211 is turned on, the transistor 217 is turned off, and the transistor 218 is turned on. Then, a signal having the same potential as the low potential power source (VSS) is outputted from the output node.

 Upon input of an L-level signal to the input node, the transistor 210 is turned on, the
15 transistor 211 is turned off, the transistor 217 is turned on, and the transistor 218 is turned off. A drain electrode of the transistor 212 has a potential which is obtained by adding the high potential power source (VDD) to the threshold voltages of the transistors 213 to 215: ($VDD + V_{THb} + V_{THb} + V_{THb}$), and this potential is supplied to a gate electrode of the transistor 216. Then, a source electrode of the transistor 216 has a potential value of ($VDD + V_{THb} + V_{THb}$),
20 and a signal having the potential of ($VDD + V_{THb} + V_{THb}$) is outputted from the output node.

A semiconductor device having a different configuration from the aforementioned includes transistors 220 to 234 (see FIG. 11). The transistors 220, 222, 226 to 229, 232 and 234 are p-channel transistors while the transistors 221, 223 to 225, 230, 231 and 233 are n-channel transistors.

25 Description is made on the operation of the semiconductor device having the aforementioned configuration. In the description below, all the transistors 223 to 225 and 231 have the same threshold voltage value ($|V_{THa}|$), while all the transistors 226 to 229 and 234 have the same threshold voltage value ($|V_{THb}|$).

 Upon input of an H-level signal to the input node, the transistor 220 is turned off, the
30 transistor 221 is turned on, the transistor 232 is turned off, and the transistor 222 is turned on.

A drain electrode of the transistor 230 has a potential which is obtained by subtracting the threshold voltages of the transistors 226 to 229 from the high potential power source (VDD): $(VDD - |V_{THa}| - |V_{THa}| - |V_{THa}| - |V_{THa}|)$, and this potential is supplied to a gate electrode of the transistor 234. Since a drain electrode of the transistor 234 has the same potential as the low potential power source (0 V), and a source electrode of the transistor 234 has a potential value of $(VDD - |V_{THa}| - |V_{THa}| - |V_{THa}|)$, a signal having the potential of $(VDD - |V_{THa}| - |V_{THa}| - |V_{THa}|)$ is outputted from the output node.

Upon input of an L-level signal to the input node, the transistor 220 is turned on, the transistor 221 is turned off, the transistor 232 is turned on, and the transistor 222 is turned off. A drain electrode of the transistor 222 has a potential which is obtained by adding the high potential power source (VDD) to the threshold voltages of the transistors 223 to 225: $(VDD + V_{THb} + V_{THb} + V_{THb})$, and this potential is supplied to a gate electrode of the transistor 231. Then, a source electrode of the transistor 231 has a potential value of $(VDD + V_{THb} + V_{THb})$, and a signal having a potential of $(VDD + V_{THb} + V_{THb})$ is outputted from the output node.

Note that each of the transistors 203 to 305, the transistors 213 to 215, the transistors 223 to 225, and the transistors 226 to 229 is a transistor of which gate electrode and drain electrode are connected to each other. These transistors are provided in order to generate a potential lower or higher than the high potential power source, and the number of such transistors is not specifically limited.

Embodiment Mode 5

Description is made with reference to FIGS. 12A and 12B on a configuration of a potential generating circuit which is a component of the invention.

The potential generating circuit 14 includes switches 51 and 52, capacitors 53 and 54 and a circuit 55 (see FIG. 12A). The switches 51 and 52 are the elements having a switching function, such as transistors or analog switches. The circuit 55 is a circuit having high input impedance such as a buffer amplifier, where a potential inputted to an input node is equal to a potential outputted from an output node. The buffer amplifier has three terminals of an input terminal, an inverting input terminal and an output terminal. The inverting input terminal and the output terminal are connected to each other.

One node of the switch 51 is connected to a high potential power source (VDD) for generating potentials. The other node of the switch 51 is connected to one node of the switch 52 and one node of the capacitor 53. The other node of the switch 52 is connected to one node of the capacitor 54 and the input node of the circuit 55. The other node of the capacitor 54 is
5 connected to the low potential power source (VSS). The other node of the capacitor 53 receives a subtraction signal (Sig). The switch 51 receives a signal having a potential (V1) while the switch 52 receives a signal having a potential (V2).

Next, description is made on the operation of the potential generating circuit 14 having the aforementioned configuration (see FIG. 12B). Note that the switches 51 and 52 are turned
10 on (become conductive) upon receiving an H-level signal (VH) while they are turned off (become non-conductive) upon receiving an L-level signal (VL).

In a period (period T1) in which the switch 51 is on, the switch 52 is off, and a potential of the subtraction signal is at Va, a potential of the connecting node of the switches 51 and 52 drops gradually from the high potential power source (VDD) for generating potentials toward a
15 potential of $(VDD - (Va - VSS))$.

Next, in a period (period T2) in which the switch 51 is off, the switch 52 is on, and a potential of the subtraction signal is at Va, the operation in the period T1 is still carried on, and thus the potential of the connecting node of the switches 51 and 52 drops gradually from the high potential power source (VDD) for generating potentials toward the potential of $(VDD - (Va -$
20 $VSS))$. When the potential of the subtraction signal changes from Va to VSS, the potential of the connecting node of the switches 51 and 52 becomes $(VDD - (Va - VSS))$.

Then, in a period (period T3) in which the switch 51 is off, the switch 52 is on, and a potential of the subtraction signal is at VSS, the potential generated in the period T2 $(VDD - (Va -$
25 $VSS))$ is inputted to the input node of the circuit 55. Then, the potential of $(VDD - (Va - VSS))$ is outputted from the output node of the circuit 55.

Embodiment Mode 6

Description is made with reference to FIG. 13 on a configuration of a potential generating circuit which is a component of the semiconductor device of the invention.

30 The potential generating circuit 14 has multiple resistors connected in series. One end

of the multiple resistors connected in series is connected to the high potential power source (VDD) while the other end thereof is connected to the low potential power source (VSS). The potential generating circuit 14 outputs potentials from a connecting node of two resistors that are selected from among the multiple resistors. The aforementioned configuration corresponds to a circuit utilizing resistance division, in which a new potential is generated by utilizing a potential of the high potential power source or the low potential power source.

In the shown configuration, the potential generating circuit 14 has resistors 56 and 57 connected in series. One node of the resistor 56 is connected to the high potential power source, and one node of the resistor 57 is connected to the low potential power source. A potential is outputted from a connecting node of the other node of the resistor 56 and the other node of the resistor 57.

Embodiment Mode 7

Description is made with reference to FIG. 21 on a configuration of the potential generating circuit 14 which is a component of of the invention.

The potential generating circuit 14 includes power sources 301 to 303, transistors 304 to 310, and resistors 312 to 314. The power sources 301 and 302 are fixed power sources while the power source 303 is a variable power source. The transistors 304, 307 and 308 are p-channel transistors while the transistors 305, 306, 309 and 310 are n-channel transistors.

The transistors 305 and 306, the transistors 307 and 308, and the transistors 309 and 310 each are current mirror circuits. The two transistors which are a current mirror circuit have the same current value.

The power source 301 outputs a potential V_a , the power source 302 outputs a potential V_b , and the power source 303 outputs a potential V_c (the potentials V_a and V_b satisfy $V_a > V_b$).

Description is made below on the operation of the potential generating circuit 14 having the aforementioned configuration. In the description below, all the transistors 304, 307 and 308 have the same threshold voltage value (V_{THa}) while all the transistors 305, 306, 309 and 310 have the same threshold voltage value (V_{THb}). In addition, the resistance values of the resistors 312 and 313 are each R_1 while the resistance value of the resistor 314 is R_2 .

Since a gate electrode of the transistor 304 has the same level as the potential V_b , a

drain electrode of the transistor 304 has a potential which is obtained by adding the potential V_b to the threshold voltage: $(V_b + |V_{THa}|)$. In addition, since a source electrode of the transistor 307 has the level as the potential V_b , drain and gate electrodes of the transistor 307 have a potential which is obtained by subtracting the threshold voltage from the potential V_b : $(V_b - |V_{THa}|)$. Further, since a gate electrode of the transistor 308 has a potential of $(V_b - |V_{THa}|)$, a source electrode of the transistor 308 has a potential V_b which is obtained by subtracting the threshold voltage from the potential of the gate electrode.

One node of the resistor 313 receives the potential V_a while the other node thereof receives the potential V_b , and thus the resistor 313 has a current value obtained by subtracting the potential V_b from the potential V_a and then dividing it by the resistance value R_1 : $((V_a - V_b)/R_1)$.

The resistor 313 and the transistors 309 and 310 have the same current value. Since one node of the resistor 314 has a potential of V_c , the other node of the resistor 314 has a potential of $(V_c - (V_a - V_b) \times R_2/R_1)$.

In this manner, the potential generating circuit 14 can generate a new potential $(V_c - (V_a - V_b) \times R_2/R_1)$ which is different from the potentials V_a and V_b . In addition, since a potential generated by the potential generating circuit 14 has no relation to the threshold voltage value of transistors, it is not affected by variations in the threshold voltage of the transistors.

Embodiment Mode 8

Description is made with reference to FIG. 22 on a signal output circuit which is a component of of the invention.

The signal output circuit includes transistors 360 to 364 and the potential generating circuit 14. The transistors 360 to 362 and 364 are n-channel transistors while the transistor 363 is a p-channel transistor. The signal output circuit outputs a signal from its output node upon input of a signal to an input node thereof.

Description is made with reference to FIG. 22 on the potential generating circuit 14.

The potential generating circuit 14 includes power sources 321 to 325, transistors 340 to 359, and resistors 371 to 375. The power sources 321 and 322 are fixed power sources while the power sources 323 to 325 are variable power sources. The transistors 340, 343, 344 and

350 to 359 are p-channel transistors while the transistors 341, 342 and 346 to 369 are n-channel transistors. The transistors 341 and 342, the transistors 343 and 344, the transistors 345 to 349, the transistors 350 and 353, the transistors 351 and 354, the transistors 352 and 355, and the transistors 356 to 359 each are current mirror circuits. The two transistors which are a
5 current mirror circuit have the same current value.

The power source 321 outputs a potential V_a , the power source 322 outputs a potential V_b , the power source 323 outputs a potential V_c , the power source 324 outputs a potential V_d , and the power source 325 outputs a potential V_e (the potentials V_a and V_b satisfy $V_a > V_b$).

Description is made below on the operation of the potential generating circuit 14 having
10 the aforementioned configuration. In the description below, all the p-channel transistors have the same threshold voltage value ($|V_{THa}|$) while all the n-channel transistors have the same threshold voltage value (V_{THb}). In addition, the resistance values of the resistors 371 and 372 are each R_1 while the resistance values of the resistors 373 to 375 are each R_2 .

Since a gate electrode of the transistor 340 has the same level as the potential V_b , a
15 drain electrode of the transistor 340 has a potential which is obtained by adding the potential V_b to the threshold voltage ($V_b + |V_{THa}|$).

In addition, since a source electrode of the transistor 343 has the same level as the potential V_b , drain and gate electrodes of the transistor 343 have a potential which is obtained by subtracting the threshold voltage ($|V_{THa}|$) from the potential V_b : ($V_b - |V_{THa}|$).

Further, since a gate electrode of the transistor 344 has a potential of ($V_b - |V_{THa}|$), a
20 source electrode of the transistor 344 has a potential V_b which is obtained by subtracting the threshold voltage ($|V_{THa}|$) from the potential of the gate electrode ($V_b - |V_{THa}|$). One node of the resistor 372 receives the potential V_a while the other node thereof receives the potential V_b , and thus the resistor 372 has a current value obtained by subtracting the potential V_b from the
25 potential V_a and then dividing it by the resistance value R_1 : $((V_a - V_b)/R_1)$.

Since a drain electrode of the transistor 350 has the same level as the potential V_c , drain and gate electrodes of the transistor 350 have a potential of ($V_c - |V_{THa}|$). In addition, since a drain electrode of the transistor 351 has the same level as the potential V_d , drain and gate electrodes of the transistor 351 have a potential of ($V_d - |V_{THa}|$). Further, since a drain
30 electrode of the transistor 352 has the same level as the potential V_e , drain and gate electrodes of

the transistor 352 have a potential of $(V_e - |V_{THa}|)$.

Then, a source electrode of the transistor 353 has a potential of V_c . A source electrode of the transistor 354 has a potential of V_d . A source electrode of the transistor 355 has a potential of V_e .

5 Then, a gate electrode of the transistor 360 has a potential of $(V_c + I \times R_2)$, a gate electrode of the transistor 361 has a potential of $(V_d + I \times R_2)$, a gate electrode of the transistor 362 has a potential of $(V_e + I \times R_2)$ (I denotes the respective current values of the transistors 357 to 359). The potentials supplied to these transistors 360 to 362 become the output of the potential generating circuit 14.

10 In this manner, the potential generating circuit 14 can generate new potentials $(V_c + I \times R_2)$, $(V_d + I \times R_2)$ and $(V_e + I \times R_2)$ which are different from the potentials V_a to V_e . In addition, since potentials generated by the potential generating circuit 14 have no relation to the threshold voltage value of transistors, it is not affected by variations in the threshold voltage of the transistors.

15 Thus, a source electrode of the transistor 360 has a potential of $(V_c + I \times R_2 - |V_{THa}|)$, a source electrode of the transistor 361 has a potential of $(V_d + I \times R_2 - |V_{THa}|)$, and a source electrode of the transistor 362 has a potential of $(V_e + I \times R_2 - |V_{THa}|)$. According to relational expressions of $V_c > V_d$ and $V_c > V_e$, the transistor 363 is turned on while the transistor 364 is turned off when a signal inputted to the input node of the signal output circuit has an L level, and a potential of $(V_c + I \times R_2 - |V_{THa}|)$ is outputted from the output node of the signal output circuit.

Embodiment Mode 9

25 A semiconductor device of the invention includes the potential generating circuit 14 and transistors 241 to 243 (see FIGS. 23A and 23B). The potential generating circuit 14 has a resistor 244 and a transistor 245 (see FIG. 23A). In addition, the potential generating circuit 14 having a different configuration from the aforementioned includes a resistor 244 and transistors 245 and 246 (see FIG. 23B).

30 The transistors 241, 242 and 246 are n-channel transistors while the transistors 243 and 245 are p-channel transistors. A predetermined voltage (V_a) is applied to a gate of the transistor

245, and the transistor 245 operates in the saturation region. Additionally, the transistor 245 operates as a constant current source. The potential generating circuit 14 generates a potential V_c which is different from the potentials of the high potential power source (VDD) and the low potential power source (VSS) ($VSS < V_c < VDD$).

5 If an H-level signal is inputted to an input node, the transistor 241 is turned off while the transistor 243 is turned on. Then, an output node outputs a potential ($V_c + |V_{THa}|$) which is obtained by adding the output potential V_c of the potential generating circuit 14 to the threshold voltage ($|V_{THa}|$) of the transistor 242.

Meanwhile, if an L-level signal is inputted to the input node, the transistor 241 is turned on while the transistor 243 is turned off, and a potential of the high potential power source (VDD) is outputted from the output node.

In this manner, in the semiconductor device of the invention, a potential difference between two signals outputted from an output node can be controlled to be smaller than a potential difference between the high potential power source and the low potential power source.

15 Accordingly, the power consumption can be reduced.

Embodiment 1

Description is made with reference to FIG. 14 on a configuration of a semiconductor device of the invention. The semiconductor device of the invention includes the source driver

20 101, the gate driver 106 and the pixel portion 109.

The source driver 101 includes a pulse output circuit 102, latch circuits 103 and 104, and a buffer circuit 105. The gate driver 106 includes a pulse output circuit 107 and a buffer circuit 108. The pulse output circuits 102 and 107 are circuits for outputting sampling pulses, such as shift registers or decoders. The latch circuits 103 and 104 hold video signals and

25 outputs the video signals to a circuit of a lower stage. The buffer circuits 105 and 108 each include the multiple signal output circuits 10.

The pixel portion 109 has multiple (x , where x is a natural number) source lines (S_1 to S_x), multiple (y , where y is a natural number) gate lines (G_1 to G_y), multiple power source lines (V_1 to V_x), and multiple pixels 110.

30 Each of the multiple pixels 110 has an n-channel transistor 112, a p-channel transistor

113 and a light-emitting element 111. The n-channel transistor 112 is a switching transistor for controlling input of video signals to the pixel 110. The p-channel transistor 113 is a driving transistor for controlling current supply to the light-emitting element 111 in accordance with a potential of the video signal inputted to the pixel 110. One electrode of the light-emitting
5 element 111 is connected to the high potential power source (VDD) through the p-channel transistor 113 while the other electrode thereof is connected to the low potential power source (VSS). Therefore, the amount of current supplied to the light-emitting element 111 is determined by a potential difference between the high potential power source and the low potential power source.

10 Note that the configuration of the pixel 110 is not limited to the aforementioned, and a capacitor may be provided for holding a gate-source voltage of the p-channel transistor 113. Further, each of the switching transistor and the driving transistor is not limited to the aforementioned conductivity type, and either an n-channel or p-channel transistor may be employed.

15 In the case of expressing gray scales by using a semiconductor device, there is a method of using analog video signals or a method of using digital video signals. In the former method, gray scales are expressed by controlling the luminance of light-emitting elements with analog video signals. As the latter method, there is a time gray scale method or an area gray scale method. The invention may adopt either of the methods.

20 In the invention, the p-channel transistor 113 is operated in the linear region and constant voltage drive is performed in which a constant voltage is applied to the light-emitting element 111. In comparison with constant current drive, the constant voltage drive does not require the p-channel transistor 113 to operate in the saturation region; therefore, a driving voltage is not required to be increased. Accordingly, the power consumption can be reduced as
25 compared to the constant current drive.

In the aforementioned configuration, the signal output circuits 10 are provided in the source driver 101, and two signals inputted to the p-channel transistor 113 have a potential difference which can certainly turn on or off the p-channel transistor 113 which is operated in the linear region. In addition, this potential difference is smaller than a potential difference
30 between the high potential power source and the low potential power source. In this manner, in

the invention, a potential difference between two signals inputted to the p-channel transistor 113 can be controlled to be smaller than a potential difference between the high potential power source and the low potential power source. Accordingly, the power consumption can be reduced. This embodiment can be appropriately implemented in combination with the
5 aforementioned embodiment modes.

Embodiment 2

Description is made with reference to FIG. 15 on a configuration of a semiconductor device of the invention. The semiconductor device of the invention includes the pixel portion
10 109 and a monitoring unit 152. The pixel portion 109 has multiple pixels each of which includes the light-emitting element 111 and at least two transistors. In the shown configuration, only the p-channel transistor 113 connected in series to the light-emitting element 111 is shown. One of the two electrodes of the light-emitting element 111 is connected to the low potential power source (VSS) and the other is connected to the p-channel transistor 113.

15 The light-emitting element 111 has temperature dependency, and the resistance value thereof is decreased when the ambient temperature becomes high whereas the resistance value is increased when the ambient temperature becomes low. In addition, the light-emitting element degrades with time, and the resistance value thereof is increased in accordance with the degradation with time. The luminance of a light-emitting element depends on the current value
20 supplied thereto. Therefore, if the ambient temperature changes or the light-emitting element degrades with time, the current value supplied to the light-emitting element changes, thereby the desired luminance cannot be obtained. The semiconductor device of this embodiment is characterized by having the monitoring unit 152. The monitoring element 152 has one or more monitoring light-emitting elements 157, a limiter transistor 158, a buffer amplifier 153 and a
25 constant current source 154. One of two electrodes of the monitoring light-emitting element 157 is connected to the low potential power source (VSS) and the other is connected to the limiter transistor 158. A gate electrode of the limiter transistor 158 is kept at a constant potential (VH) and thus the limiter transistor 158 is on.

The light-emitting element 111 and the monitoring light-emitting element 157 are formed
30 through the same steps with the same conditions, and have the same or substantially the same

characteristics with respect to changes in the ambient temperature and degradation with time. The light-emitting element 111 and the monitoring light-emitting element 157 are provided over the same substrate. The monitoring light-emitting element 157 is supplied with a constant current from the constant current source 154. If the ambient temperature changes or the monitoring light-emitting element 157 degrades with time in such a state, the resistance value of the monitoring light-emitting element 157 changes. Since the current value of the monitoring light-emitting element 157 is constant at all times, when the resistance value of the monitoring light-emitting element 157 changes, a potential difference between the opposite electrodes of the monitoring light-emitting element 157 changes.

In the aforementioned configuration, a potential of one electrode of the monitoring light-emitting element 157 which is connected to the low potential power source does not change while a potential of the other electrode which is connected to the constant current source 154 changes. The changed potential of the electrode of the monitoring light-emitting element 157 is supplied to the input node of the buffer amplifier 153. Then, a potential outputted from the output node of the buffer amplifier 153 is supplied to one of two electrodes of the light-emitting element 111 through the p-channel transistor 113.

In this manner, a potential supplied to the light-emitting element 111 can be changed in accordance with changes in the ambient temperature and degradation with time of the light-emitting element 111; therefore, an adverse effect of changes in the ambient temperature and degradation with time of the light-emitting element 111 can be suppressed.

Note that in a semiconductor device having the aforementioned monitoring unit 152, a potential supplied to the light-emitting element 111 is gradually increased in accordance with a degradation with time in some cases. In such a case, a potential of the high potential power source may be set higher than the normal case in advance. In this manner, if a potential of the high potential power source is set high in advance, a potential difference between the high potential power source and the low potential power source is increased correspondingly. If there is a large potential difference between the high potential power source and the low potential power source, power consumption required for charging/discharging source lines or gate lines is increased correspondingly.

However, by providing the signal output circuit of the invention in a source driver or a

gate driver, a potential difference between two signals outputted from the output node can be controlled to be smaller than a potential difference between the high potential power source and the low potential power source. Accordingly, power consumption required for charging/discharging source lines or gate lines can be reduced. That is, the signal output circuit of the invention can be effectively applied to a semiconductor device having the monitoring unit 152 as described above.

This embodiment can be appropriately implemented in combination with the aforementioned embodiment modes and embodiments.

10 Embodiment 3

Description is made with reference to FIGS. 16A to 17B on structures of the semiconductor device of the invention. The semiconductor device of the invention includes the pixel portion 109, the gate driver 106 and the source driver 101 (see FIG. 16A). The pixel portion 109 having multiple pixels each of which includes the light-emitting element 111 and the p-channel transistor 113, the gate driver 106, the source driver 101 and a connecting film 122 are provided over a substrate 120. The connecting film 122 is connected to multiple ICs.

Next, cross-sectional structures of a semiconductor device are described. The p-channel transistor 113, the light-emitting element 111 and the capacitor 124 included in the pixel portion 109, and multiple elements 125 included in the source driver 101 are formed over the substrate 120 (see FIGS. 16B, 17A and 17B).

A sealant 123 is provided around the pixel portion 109, the gate driver 106 and the source driver 101, and the light-emitting element 111 is sealed between the substrate 120 and a counter substrate 121 with the sealant 123. This sealing process is performed in order to protect the light-emitting element 111 from moisture, and a covering material (e.g., glass, ceramic, plastic or metals) is used for sealing here; however, alternatively, a sealing method using a heat curable resin or an ultraviolet curable resin, or a sealing method using a thin film with a high barrier property such as metal oxide or nitride may be employed.

If a pixel electrode of the light-emitting element 111 transmits light whereas a counter electrode thereof shields light, the light-emitting element 111 performs bottom emission (see FIG. 16B). If the pixel electrode of the light-emitting element 111 shields light whereas the counter

electrode thereof transmits light, the light-emitting element 111 performs top emission (see FIG. 17A). If both the pixel electrode and the counter electrode of the light-emitting element 111 transmit light, the light-emitting element 111 performs dual emission (see FIG. 17B).

An insulating layer may be provided over source/drain wires of the p-channel transistor 113. In such a case, the pixel electrode of the light-emitting element 111 may be provided over the insulating layer (see FIG. 16B), or in the same layer as the source/drain wires of the p-channel transistor 113 (see FIGS. 17A and 17B). In a portion where the source/drain wires of the p-channel transistor 113 and the pixel electrode of the light-emitting element 111 are stacked, the source/drain wires of the p-channel transistor 113 may be provided as the lower layer while the pixel electrode of the light-emitting element 111 may be provided as the upper layer (see FIG. 17A). Alternatively, the pixel electrode of the light-emitting element 111 may be provided as the lower layer while the source/drain wirings of the p-channel transistor 113 may be provided as the upper layer (see FIG. 17B).

Each element provided over the substrate 120 is preferably formed using a transistor which has a crystalline semiconductor with excellent characteristics such as mobility as a channel portion. Accordingly, monolithic integration over the same surface can be achieved. A semiconductor device having the aforementioned configuration has a less number of external ICs to be connected; therefore, downsizing, weight saving and thinner shape can be achieved.

Alternatively, each element provided over the substrate 120 may be formed using a transistor which has an amorphous semiconductor as a channel portion while the gate driver 106 and the source driver 101 may be constructed of IC chips. The IC chips are attached to the substrate 120 by COG bonding or attached to the connecting film 122. The amorphous semiconductor can be easily formed over a large substrate by using CVD without requiring a crystallization step; therefore, an inexpensive panel can be provided. In addition, by forming a conductive layer by a droplet discharge method typified by an ink-jet deposition method at this time, an even more inexpensive panel can be provided.

A light-emitting element included in the semiconductor device of the invention includes an element of which luminance is controlled with current or voltage, specifically such as an OLED (Organic Light Emitting Diode) or an MIM electron source element (electron-emitting element) used in an FED (Field Emission Display). An OLED as one of the light-emitting

elements includes an anode, a cathode, and a layer containing an electroluminescent material (hereinafter abbreviated as an electroluminescent layer) which emits luminescence (electroluminescence) when an electric field is applied thereto. The electroluminescent layer is provided between the anode and the cathode, and has a single layer or multiple layers. Such
5 layers may include an inorganic compound. The luminescence in the electroluminescent layer includes light emission (fluorescence) which is obtained in returning from a singlet excited state to the ground state, and light emission (phosphorescence) which is obtained in returning from a triplet excited state to the ground state. This embodiment can be appropriately implemented in combination with the aforementioned embodiment modes and embodiments.

10

Embodiment 4

Description is made with reference to FIGS. 18 to 19F on modes of an electronic appliance using the semiconductor device of the invention. An electronic appliance illustrated here is a portable phone set, which includes housings 2700 and 2706, a panel 2701, a housing
15 2702, a printed wiring board 2703, operating buttons 2704 and a battery 2705 (see FIG. 18). The panel 2701 has a pixel portion in which multiple pixels are arranged in matrix, and the pixel portion is sealed with a pair of substrates. The panel 2701 is incorporated in the housing 2702 to be attached/detached easily, and the housing 2702 is put into the printed wiring board 2703. The shape and size of the housing 2702 are appropriately changed in accordance with an
20 electronic appliance in which the panel 2701 is incorporated. Multiple IC chips which correspond to one or more of a central processing unit (CPU), a controller circuit, a power source circuit, a buffer amplifier, a source driver and a gate driver are mounted on the printed wiring board 2703. A module corresponds to a state in which the printed wiring board 2703 is mounted on the panel.

25

The panel 2701 is connected to the printed wiring board 2703 through the connecting film 2708. The panel 2701, the housing 2702 and the printed wiring board 2703 are incorporated into the housings 2700 and 2706 together with the operating button 2704 and the battery 2705. The pixel portion included in the panel 2701 is disposed so as to be seen from an open window provided in the housing 2700.

30

Note that the housings 2700 and 2706 are shown only as an illustrative external shape of

the portable phone set, and an electronic appliance in accordance with this embodiment mode can be changed into various modes in accordance with the functions or applications. Thus, description is made with reference to FIGS. 19A to 19F on exemplary modes of electronic appliances.

5 A portable phone set as a portable terminal includes a pixel portion 9102 and the like (see FIG. 19A). A portable game machine as a portable terminal includes a pixel portion 9801 and the like (see FIG. 19B). A digital video camera includes pixel portions 9701 and 9702 and the like (see FIG. 19C). A PDA (Personal Digital Assistant) as a portable information terminal includes a pixel portion 9201 and the like (see FIG. 19D). A television set includes a pixel
10 portion 9301 and the like (see FIG. 19E). A monitor device includes a pixel portion 9401 and the like (see FIG. 19F).

 The invention can be applied to various electronic appliances such as a portable terminal typified by a portable phone set (also called a portable phone device or a portable phone), a PDA, an electronic data book and a portable game machine, a television set (also called a television or
15 a television receiver), a display (also called a monitor device), a camera (e.g., a digital camera or a digital video camera), an audio reproducing device (e.g., a car audio component set), and a home-use game machine.

 This embodiment can be appropriately implemented in combination with the aforementioned embodiment modes and embodiments.

CLAIMS

1. A semiconductor device comprising:

a first transistor;

a second transistor;

5 a third transistor;

a first power source applying a first potential;

a second power source applying a second potential; and

a circuit for applying a third potential which is different from the first potential and the second potential;

10 wherein one of a source and a drain of the first transistor is connected to the first power source;

wherein the other of the source and the drain of the first transistor is connected to one of a source and a drain of the second transistor;

15 wherein the other of the source and the drain of the second transistor is connected to one of a source and a drain of the third transistor;

wherein the other of the source and the drain of the third transistor is connected to the second power source;

wherein a gate of the third transistor is connected to the circuit;

wherein a first signal is inputted to gates of the first transistor and the second transistor;

20 and

wherein a second signal is outputted from the other of the source and the drain of the first transistor and the one of the source and the drain of the second transistor.

2. The semiconductor device according to claim 1, wherein the first transistor is a p-channel transistor, the second transistor is an n-channel transistor, and the third transistor is a p-channel transistor.

3. A semiconductor device comprising:

a first transistor;

30 a second transistor;

a third transistor;

a first power source applying a first potential;

a second power source applying a second potential; and

a circuit for generating a third potential which is different from the first potential and the

5 second potential;

wherein one of a source and a drain of the third transistor is connected to the first power source;

wherein the other of the source and the drain of the third transistor is connected to one of a source and a drain of the first transistor;

10 wherein the other of the source and the drain of the first transistor is connected to one of a source and a drain of the second transistor;

wherein the other of the source and the drain of the second transistor is connected to the second power source;

wherein a gate of the third transistor is connected to the circuit;

15 wherein a first signal is inputted to gates of the first transistor and the second transistor; and

wherein a second signal is outputted from the other of the source and the drain of the first transistor and the one of the source and the drain of the second transistor.

20 4. The semiconductor device according to claim 3, wherein the first transistor is a p-channel transistor, the second transistor is an n-channel transistor, and the third transistor is an n-channel transistor.

5. A semiconductor device comprising:

25 a first transistor;

a second transistor;

a third transistor;

a fourth transistor;

a first power source applying a first potential;

30 a second power source applying a second potential;

a first circuit for generating a third potential which is different from the first potential and the second potential; and

a second circuit for generating a fourth potential which is different from the first potential and the second potential;

5 wherein one of a source and a drain of the fourth transistor is connected to the first power source;

wherein the other of the source and the drain of the fourth transistor is connected to one of a source and a drain of the first transistor;

10 wherein the other of the source and the drain of the first transistor is connected to one of a source and a drain of the second transistor;

wherein the other of the source and the drain of the second transistor is connected to one of a source and a drain of the third transistor;

wherein the other of the source and the drain of the third transistor is connected to the second power source;

15 wherein a gate of the third transistor is connected to the first circuit;

wherein a gate of the fourth transistor is connected to the second circuit;

wherein a first signal is inputted to gates of the first transistor and the second transistor; and

20 wherein a second signal is outputted from the other of the source and the drain of the first transistor and the one of the source and the drain of the second transistor.

6. The semiconductor device according to claim 5, wherein the first transistor is a p-channel transistor, the second transistor is an n-channel transistor, the third transistor is a p-channel transistor, and the fourth transistor is an n-channel transistor.

25

7. A semiconductor device comprising:

a first transistor;

a second transistor;

a third transistor;

30 a fourth transistor;

a first power source applying a first potential;
a second power source applying a second potential; and
a circuit for generating a third potential which is different from the first potential and the
second potential;

5 wherein one of a source and a drain of the first transistor and one of a source and a drain
of the third transistor is connected to the first power source;

wherein the other of the source and the drain of the first transistor is connected to one of
a source and a drain of the second transistor;

10 wherein the other of the source and the drain of the second transistor is connected to the
second power source;

wherein a gate of the second transistor is connected to the other of the source and the
drain of the third transistor and to one of a source and a drain of the fourth transistor;

wherein the other of the source and the drain of the fourth transistor is connected to the
circuit;

15 wherein a first signal is inputted to gates of the first transistor, the third transistor and
the fourth transistor; and

wherein a second signal is outputted from the other of the source and the drain of the
first transistor and the one of the source and the drain of the second transistor.

20 8. The semiconductor device according to claim 7, wherein the first transistor is a
p-channel transistor, the second transistor is a p-channel transistor, the third transistor is a
p-channel transistor, and the fourth transistor is an n-channel transistor.

9. A semiconductor device comprising:

25 a first transistor;

a second transistor;

a third transistor;

a fourth transistor;

a first power source applying a first potential;

30 a second power source applying a second potential; and

a circuit for generating a third potential which is different from the first potential and the second potential;

wherein one of a source and a drain of the first transistor is connected to the first power source;

5 wherein the other of the source and the drain of the first transistor is connected to one of a source and a drain of the second transistor;

wherein the other of the source and the drain of the second transistor and one of a source and a drain of the third transistor is connected to the second power source;

10 wherein a gate of the first transistor is connected to the other of the source and the drain of the third transistor and to one of a source and a drain of the fourth transistor;

wherein the other of the source and the drain of the fourth transistor is connected to the circuit;

wherein a first signal is inputted to gates of the second transistor, the third transistor and the fourth transistor; and

15 wherein a second signal is outputted from the other of the source and the drain of the first transistor and the one of the source and the drain of the second transistor.

10. The semiconductor device according to claim 9, wherein the first transistor is an n-channel transistor, the second transistor is an n-channel transistor, the third transistor is an n-channel transistor, and the fourth transistor is a p-channel transistor.

11. A semiconductor device comprising:

a first transistor;

a second transistor;

25 a third transistor;

a fourth transistor;

a fifth transistor;

a sixth transistor;

a first power source applying a first potential;

30 a second power source applying a second potential;

a first circuit for generating a third potential which is different from the first potential and the second potential; and

a second circuit for generating a fourth potential which is different from the first potential and the second potential;

5 wherein one of a source and a drain of the first transistor and one of a source and a drain of the third transistor is connected to the first power source;

wherein the other of the source and the drain of the first transistor is connected to one of a source and a drain of the second transistor;

10 wherein the other of the source and the drain of the second transistor and one of a source and a drain of the fifth transistor is connected to the second power source;

wherein a gate of the second transistor is connected to the other of the source and the drain of the third transistor and to one of a source and a drain of the fourth transistor;

wherein the other of the source and the drain of the fourth transistor is connected to the first circuit;

15 wherein a gate of the first transistor is connected to the other of the source and the drain of the fifth transistor and to one of a source and a drain of the sixth transistor;

wherein the other of the source and the drain of the sixth transistor is connected to the second circuit;

20 wherein a first signal is inputted to gates of the third transistor, the fourth transistor, the fifth transistor, and the sixth transistor; and

wherein a second signal is outputted from the other of the source and the drain of the first transistor and the one of the source and the drain of the second transistor.

12. The semiconductor device according to claim 11, wherein the first transistor is an
25 n-channel transistor, the second transistor is a p-channel transistor, the third transistor is a p-channel transistor, the fourth transistor is an n-channel transistor, the fifth transistor is an n-channel transistor, and the sixth transistor is a p-channel transistor.

13. A semiconductor device comprising:
30 a first transistor;

a second transistor;
a first power source applying a first potential;
a second power source applying a second potential; and
a circuit including one third transistor or multiple third transistors connected in series;
5 wherein one of a source and a drain of the first transistor is connected to the first power source;
wherein the other of the source and the drain of the first transistor is connected to one of
a source and a drain of the second transistor;
wherein the other of the source and the drain of the second transistor is connected to one
10 terminal of the circuit;
wherein the other terminal of the circuit is connected to the second power source;
wherein a gate of the third transistor is connected to a drain thereof;
wherein a first signal is inputted to gates of the first transistor and the second transistor;
and
15 wherein a second signal is outputted from the other of the source and the drain of the first transistor and the one of the source and the drain of the second transistor.

14. The semiconductor device according to claim 13, wherein the first transistor is a p-channel transistor, the second transistor is an n-channel transistor, and the third transistor is an
20 n-channel transistor.

15. A semiconductor device comprising:

a first transistor;

a second transistor;

25 a first power source applying a first potential;

a second power source applying a second potential; and

a circuit including one third transistor or multiple third transistors connected in series;

wherein one terminal of the circuit is connected to the first power source;

wherein the other terminal of the circuit is connected to one of a source and a drain of

30 the first transistor;

wherein the other of the source and the drain of the first transistor is connected to one of a source and a drain of the second transistor;

wherein the other of the source and the drain of the second transistor is connected to the second power source;

5 wherein a gate of the third transistor is connected to a drain thereof;

wherein a first signal is inputted to gates of the first transistor and the second transistor; and

wherein a second signal is outputted from the other of the source and the drain of the first transistor and the one of the source and the drain of the second transistor.

10

16. The semiconductor device according to claim 15, wherein the first transistor is a p-channel transistor, the second transistor is an n-channel transistor, and the third transistor is a p-channel transistor.

15

17. A semiconductor device comprising:

a first transistor;

a second transistor;

a first power source applying a first potential;

a second power source applying a second potential;

20

a first circuit including one third transistor or multiple third transistors connected in series; and

a second circuit including one fourth transistor or multiple fourth transistors connected in series;

wherein one terminal of the second circuit is connected to the first power source;

25

wherein the other terminal of the second circuit is connected to one of a source and a drain of the first transistor;

wherein the other of the source and the drain of the first transistor is connected to one of a source and a drain of the second transistor;

30

wherein the other of the source and the drain of the second transistor is connected to one terminal of the first circuit;

wherein the other terminal of the first circuit is connected to the second power source;

wherein a gate of the third transistor is connected to a drain thereof;

wherein a gate of the fourth transistor is connected to a drain thereof;

wherein a first signal is inputted to gates of the first transistor and the second transistor:

5 and

wherein a second signal is outputted from the other of the source and the drain of the first transistor and the one of the source and the drain of the second transistor.

18. The semiconductor device according to claim 17, wherein the first transistor is a
10 p-channel transistor, the second transistor is an n-channel transistor, the third transistor is an n-channel transistor, and the fourth transistor is a p-channel transistor.

19. The semiconductor device according to any one of claims 1, 3, 7 and 9, wherein the circuit includes multiple resistors connected in series;

15 wherein one end of the multiple resistors is connected to the first power source;

wherein the other end of the multiple resistors is connected to the second power source;

and

wherein a potential is outputted from a connecting node of two resistors that are selected from among the multiple resistors.

20

20. The semiconductor device according to any one of claims 5 and 11, wherein each of the first circuit and the second circuit include multiple resistors connected in series;

wherein one end of the multiple resistors is connected to the first power source;

wherein the other end of the multiple resistors is connected to the second power source;

25 and

wherein a potential is outputted from a connecting node of two resistors that are selected from among the multiple resistors.

21. An electronic appliance using the semiconductor device according to any one of
30 claims 1, 3, 5, 7, 9, 11, 13, 15 and 17.

1/25

FIG.1A

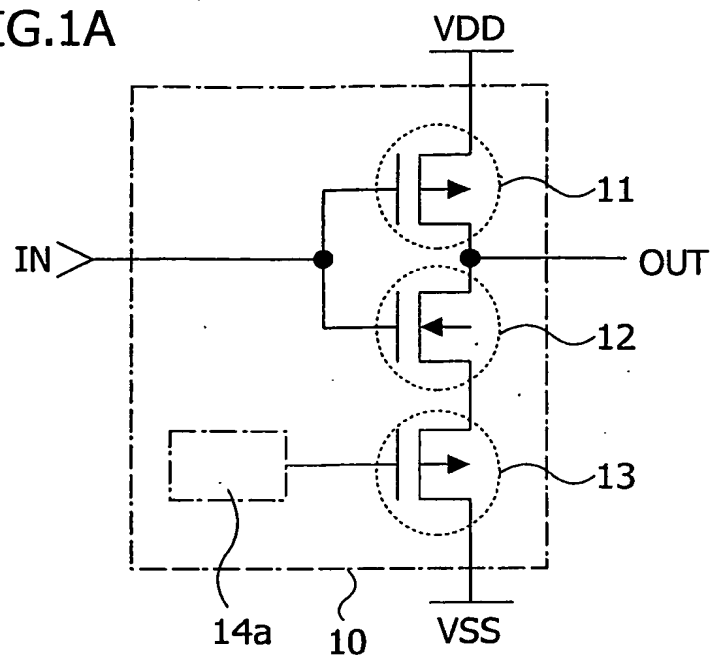
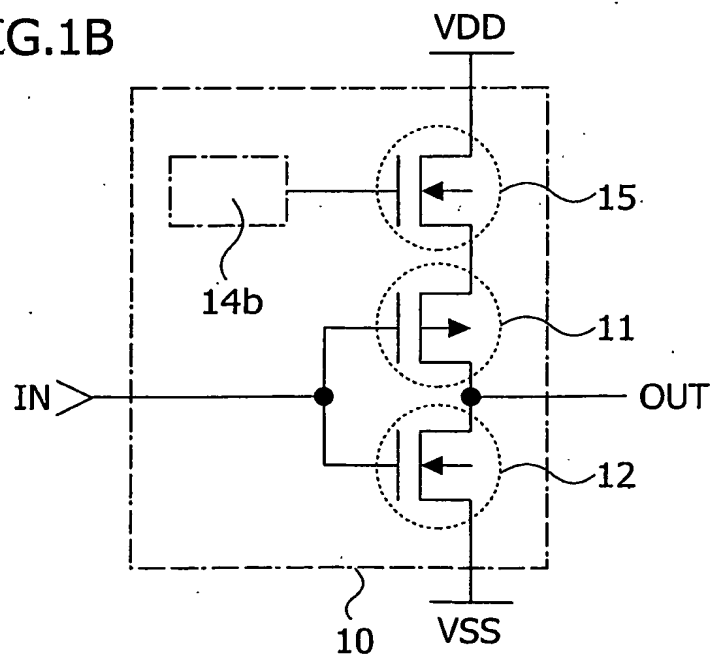


FIG.1B



2/25

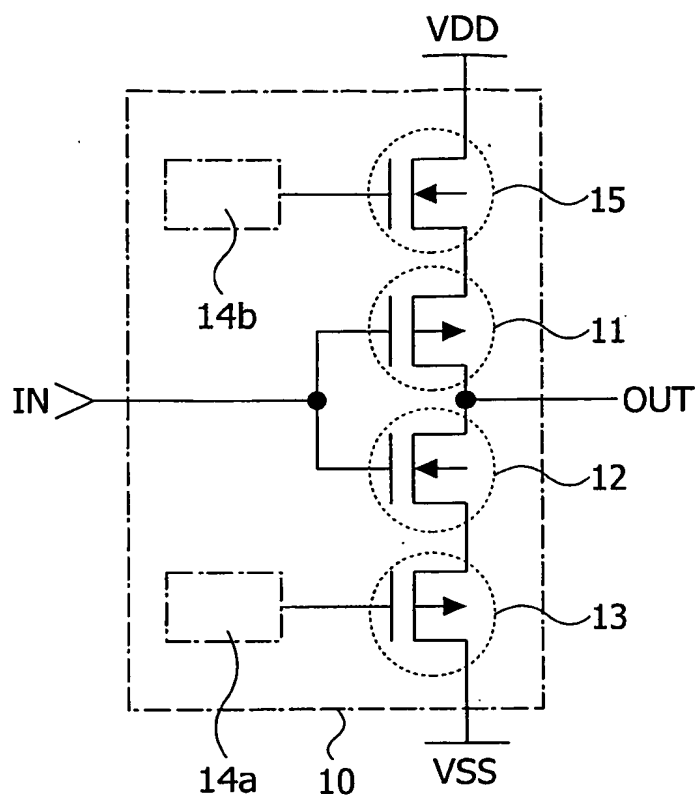


FIG.2

3/25

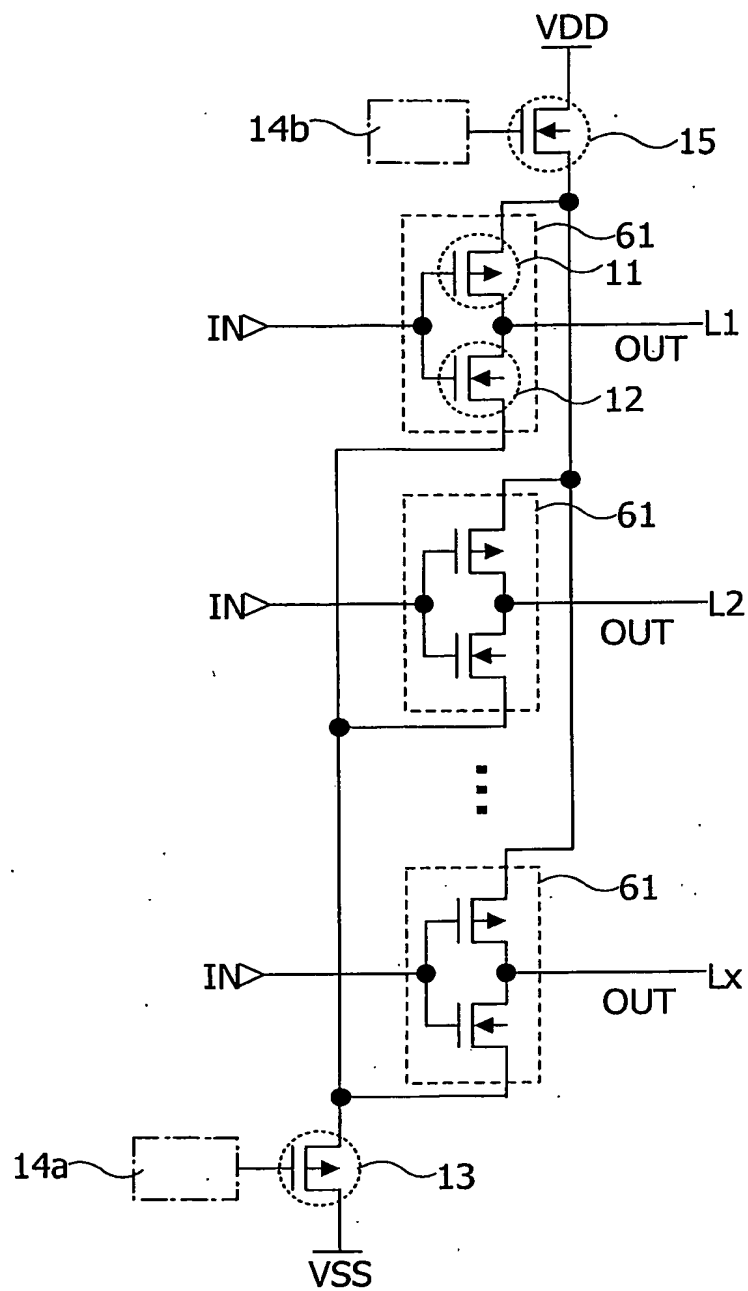
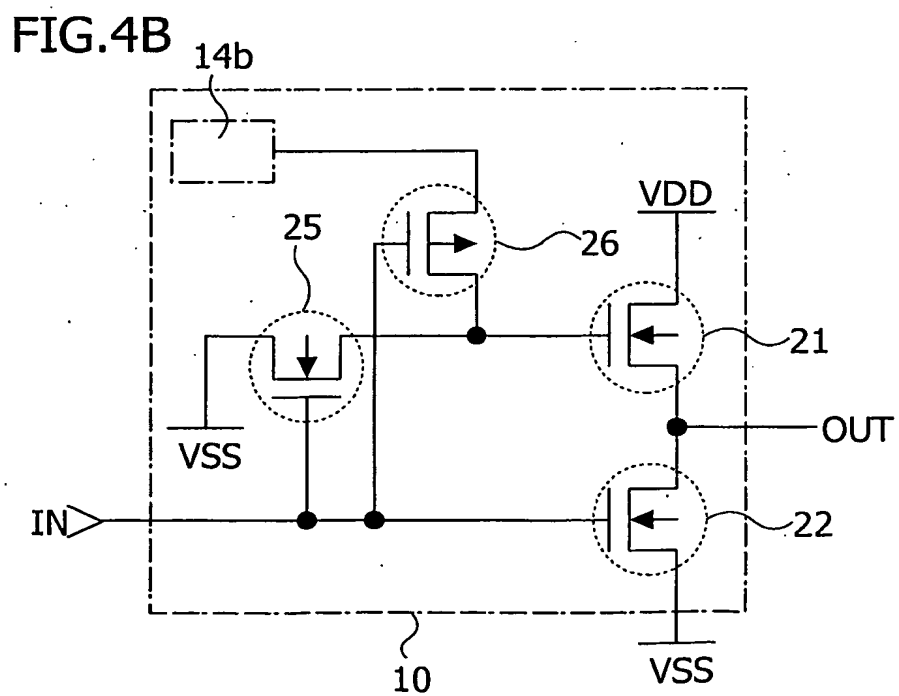
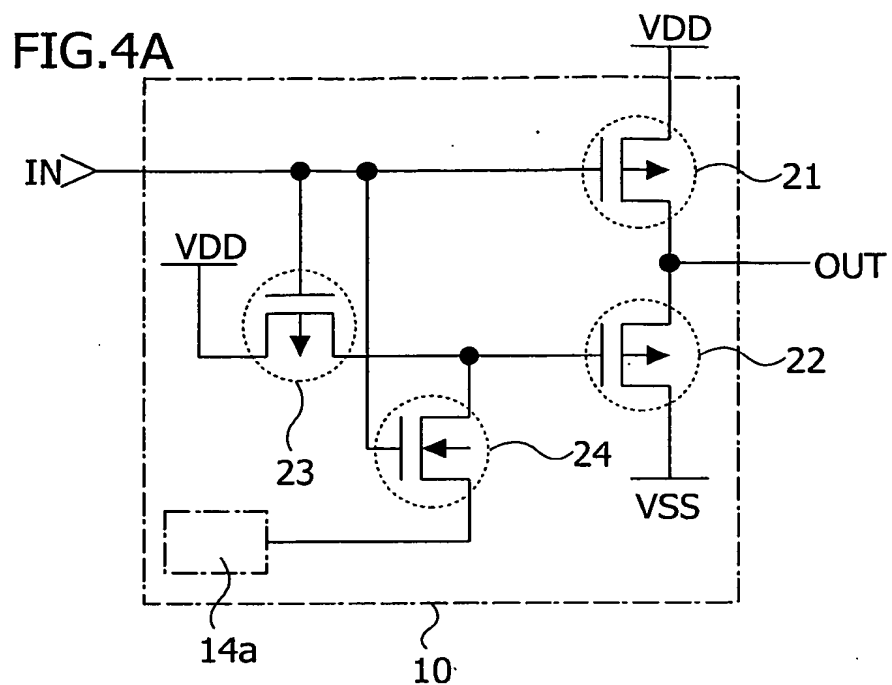


FIG.3

4/25



5/25

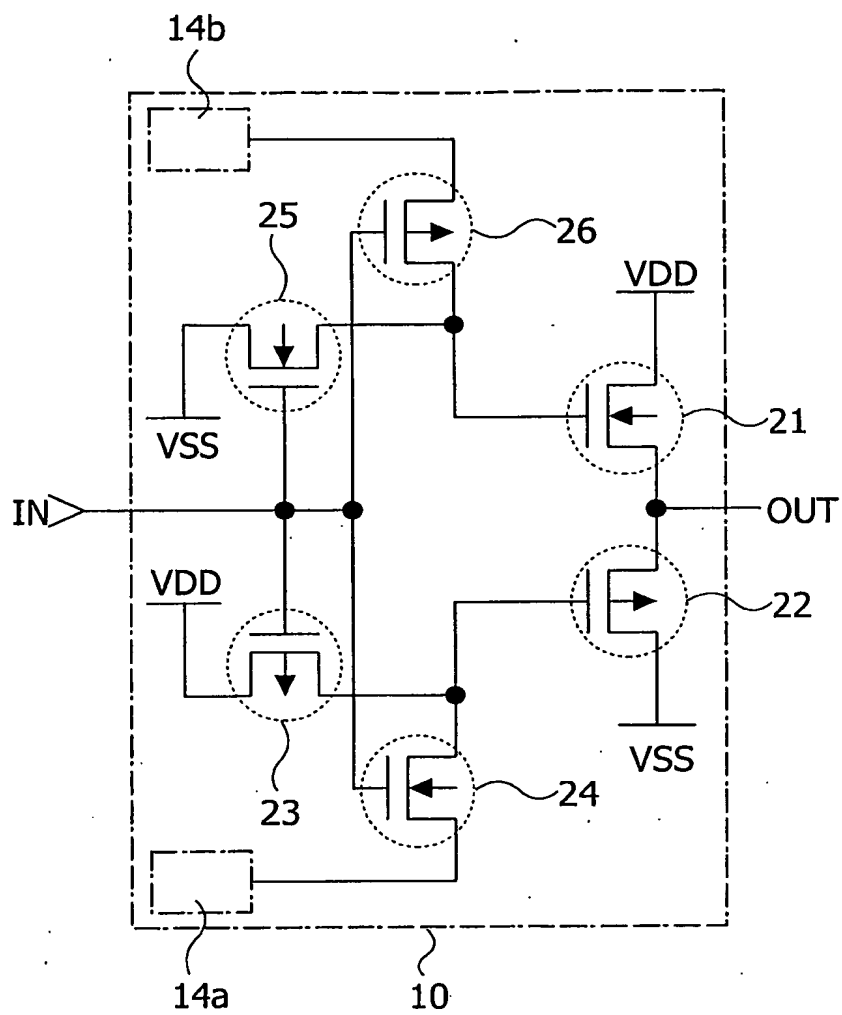
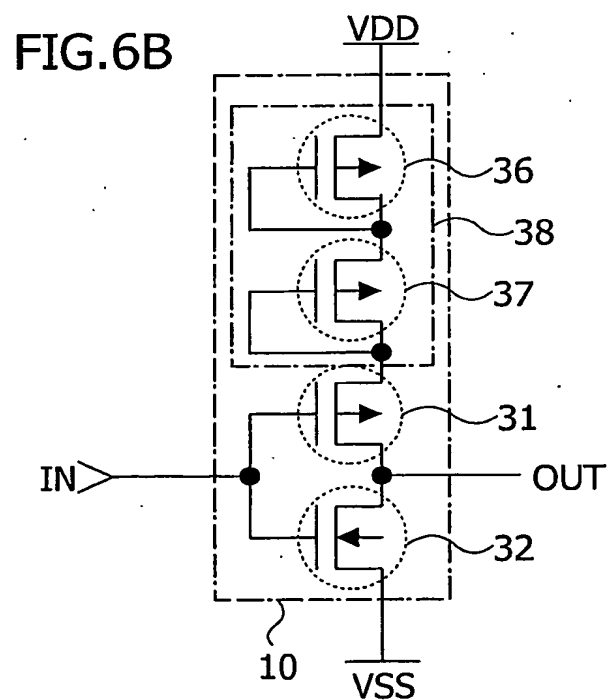
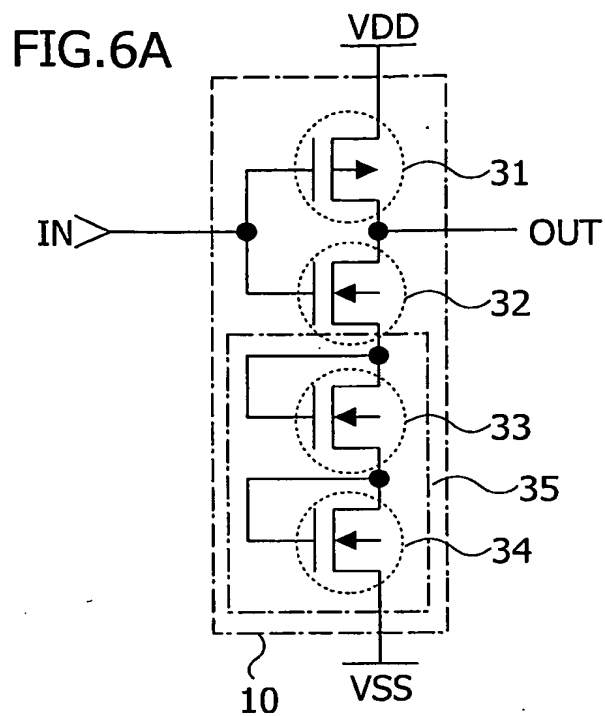


FIG.5

6/25



7/25

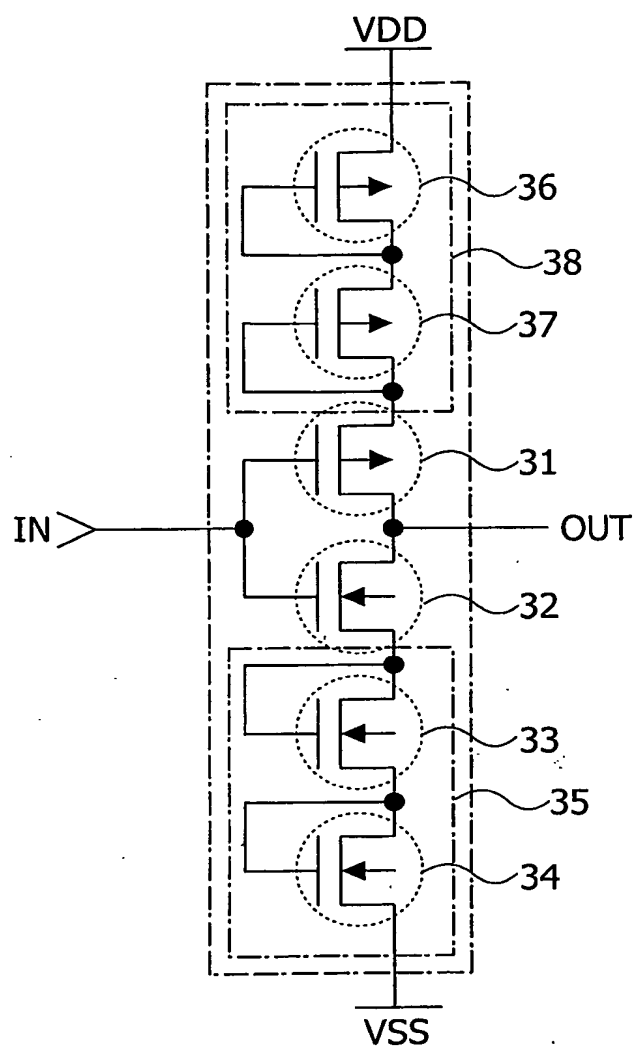


FIG.7

8/25

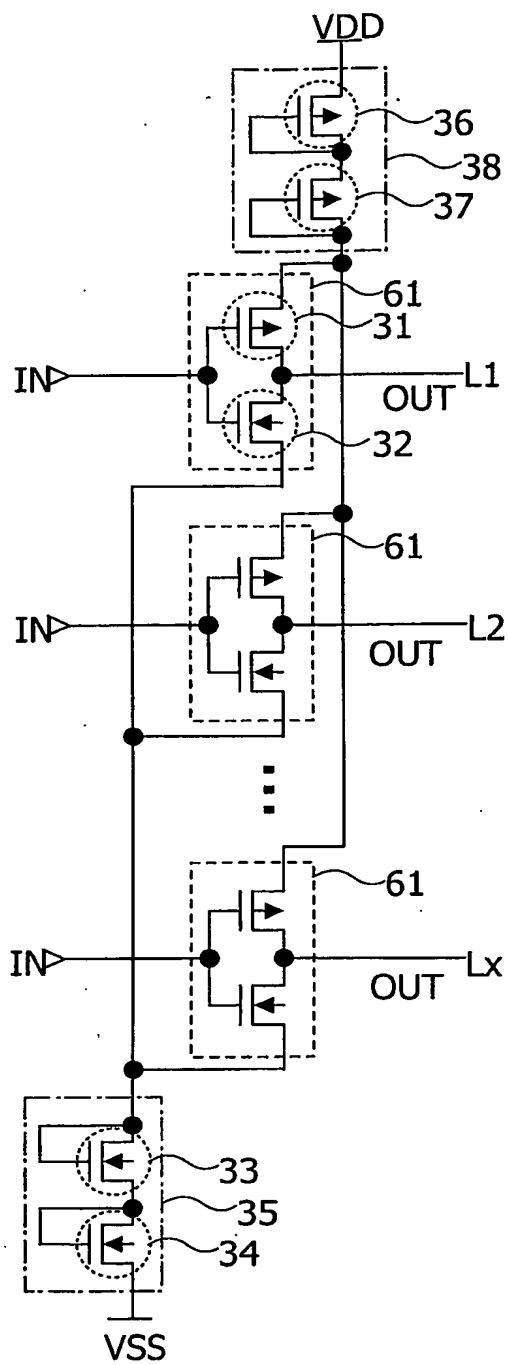


FIG.8

9/25

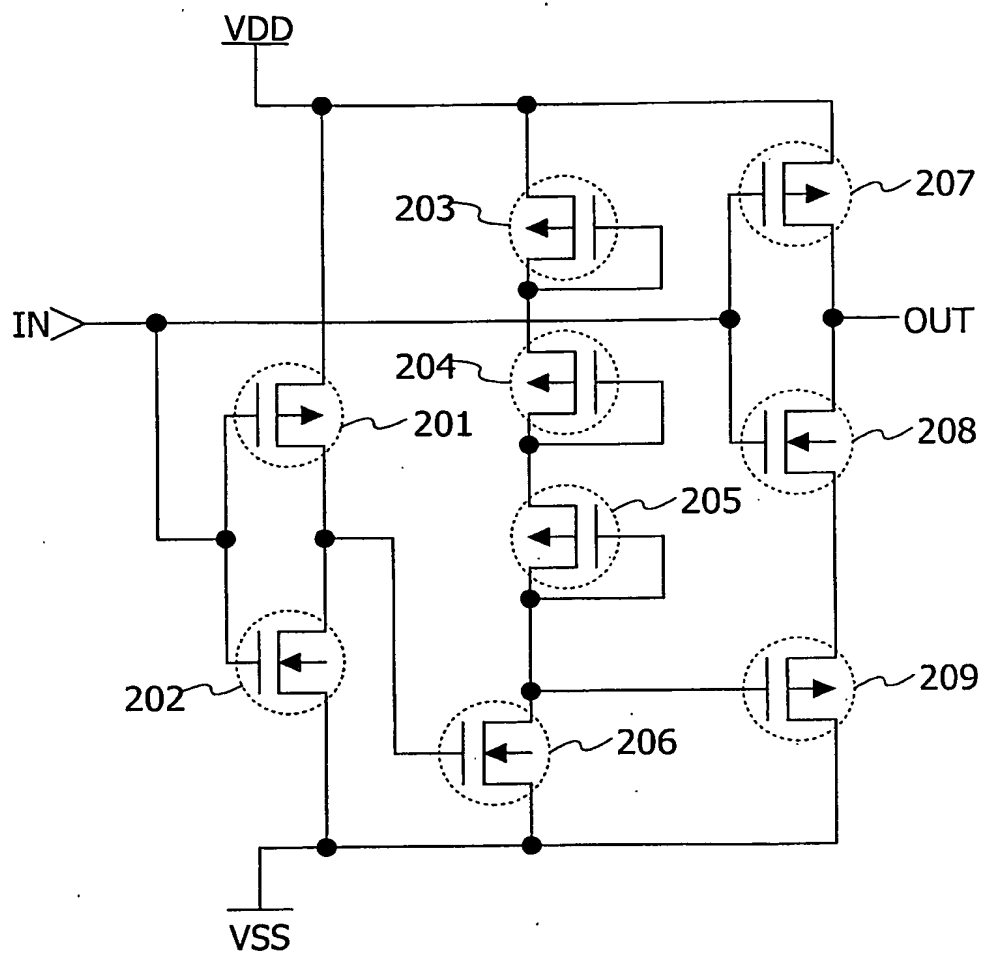


FIG.9

10/25

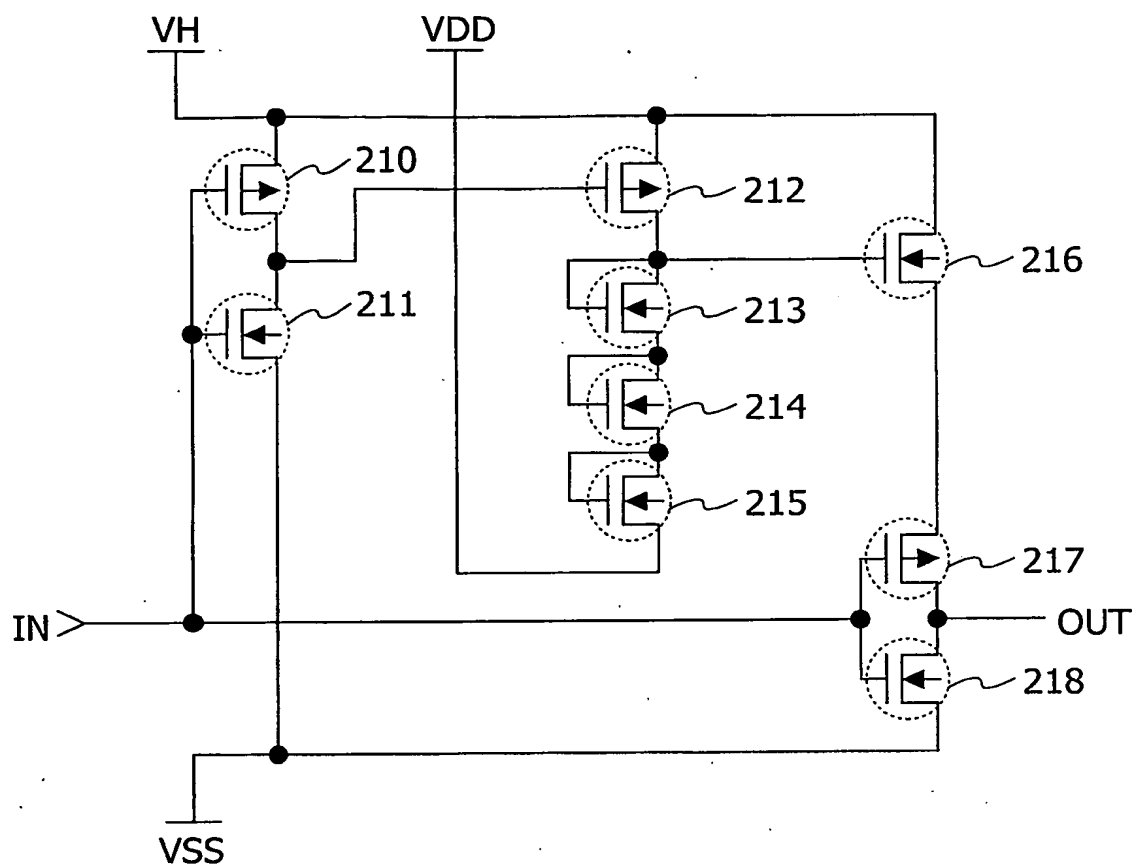


FIG.10

11/25

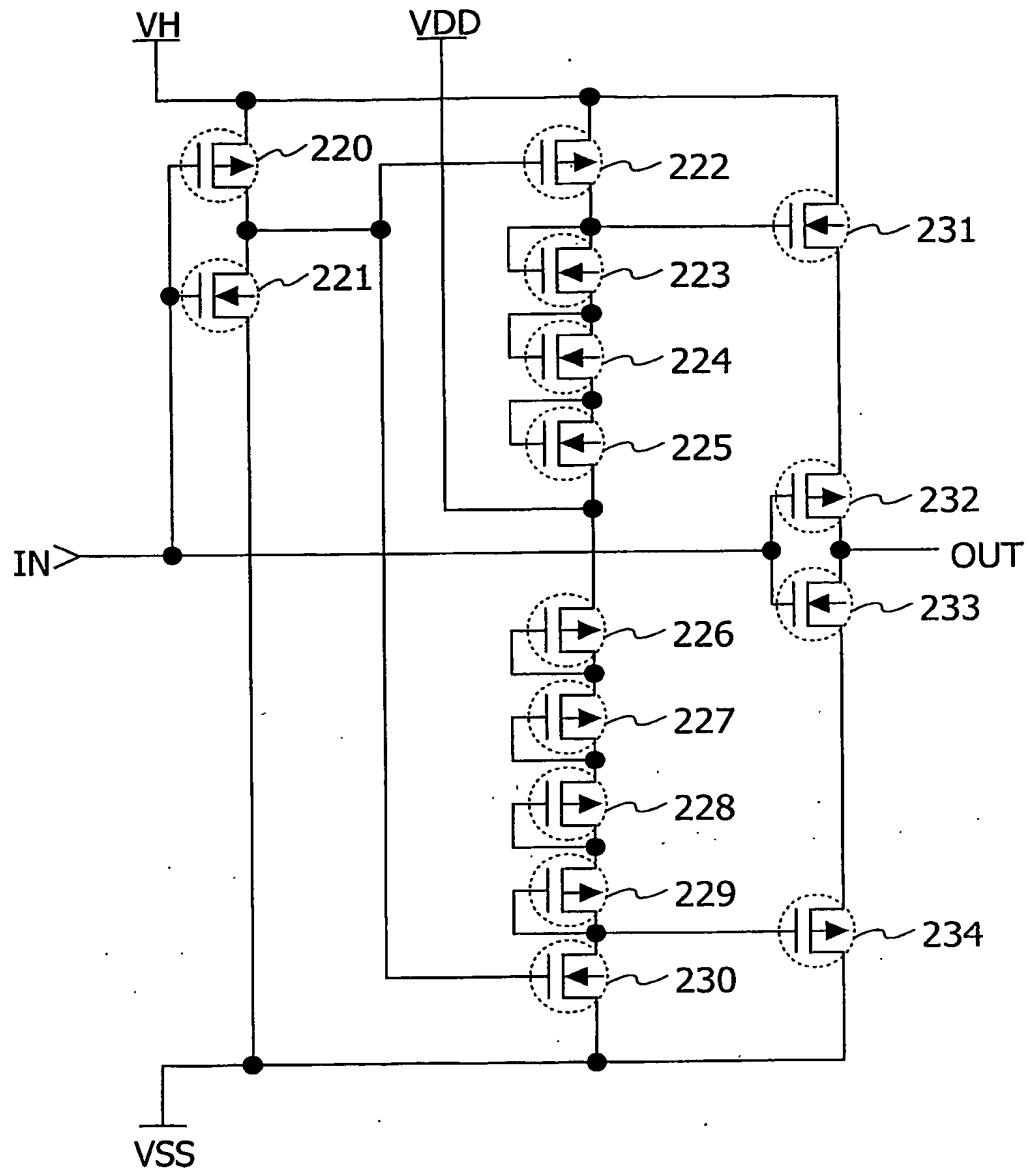


FIG.11

12/25

FIG.12A

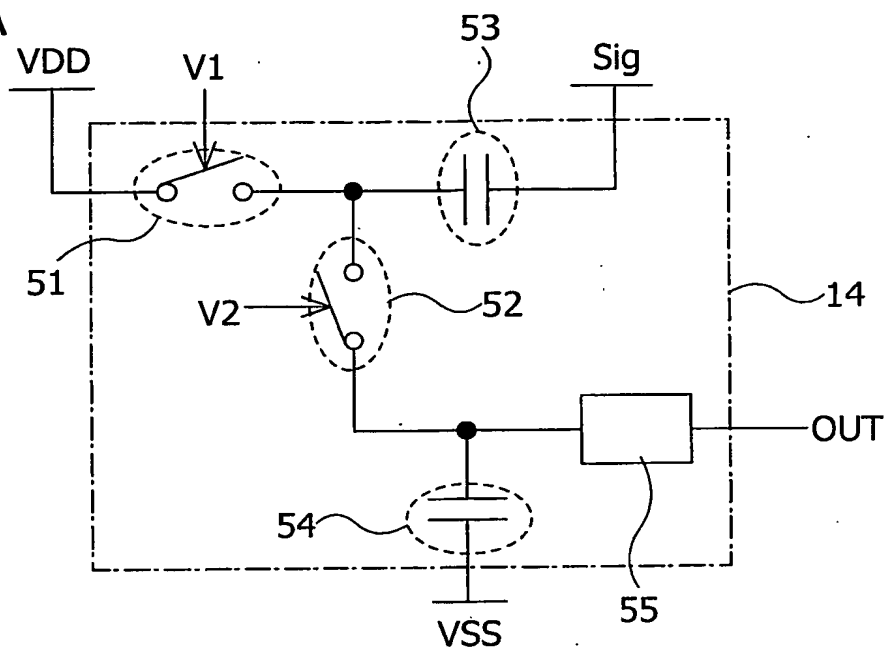
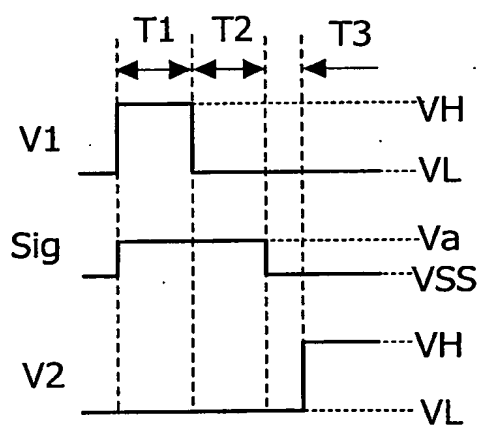


FIG.12B



13/25

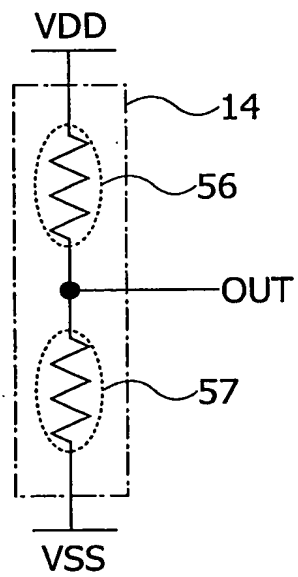


FIG.13

14/25

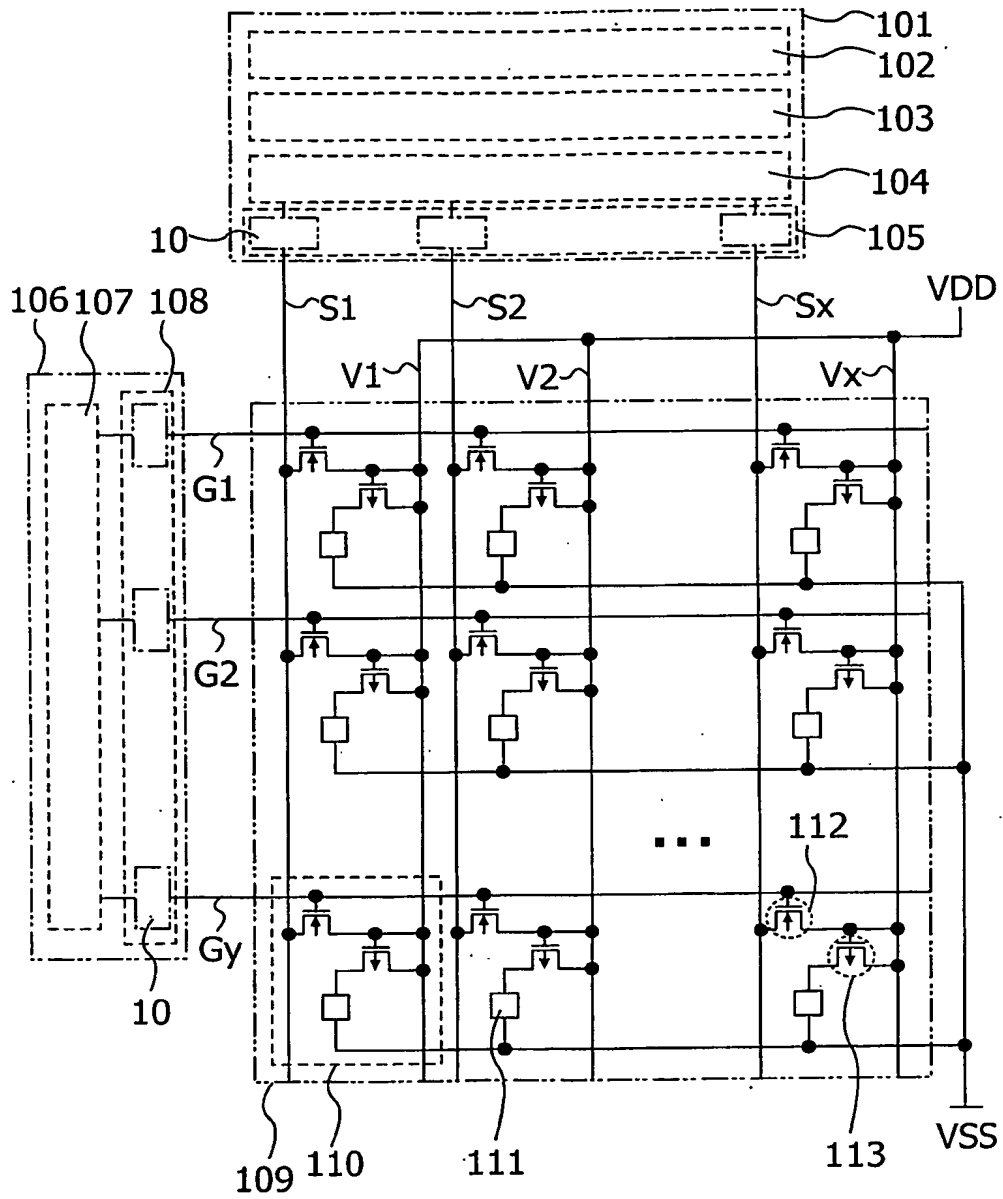


FIG.14

15/25

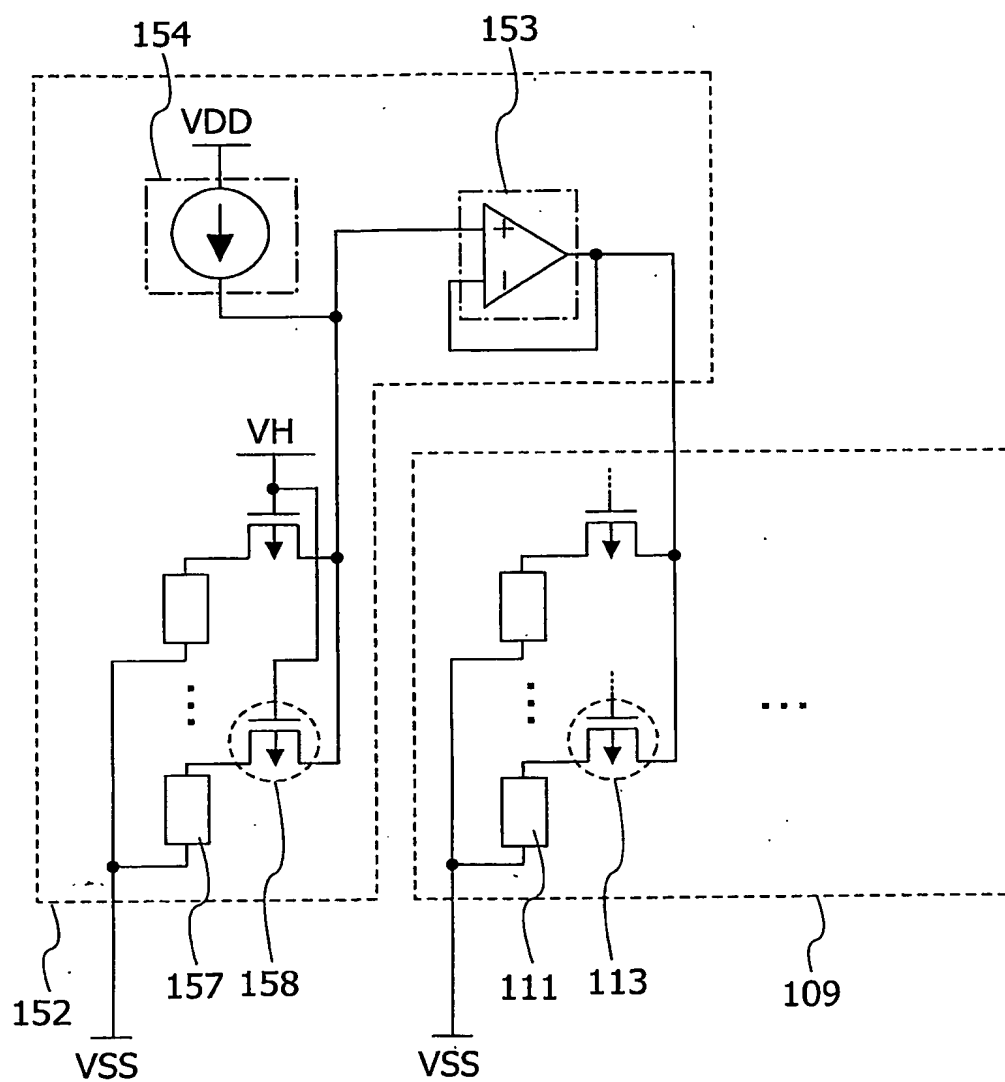
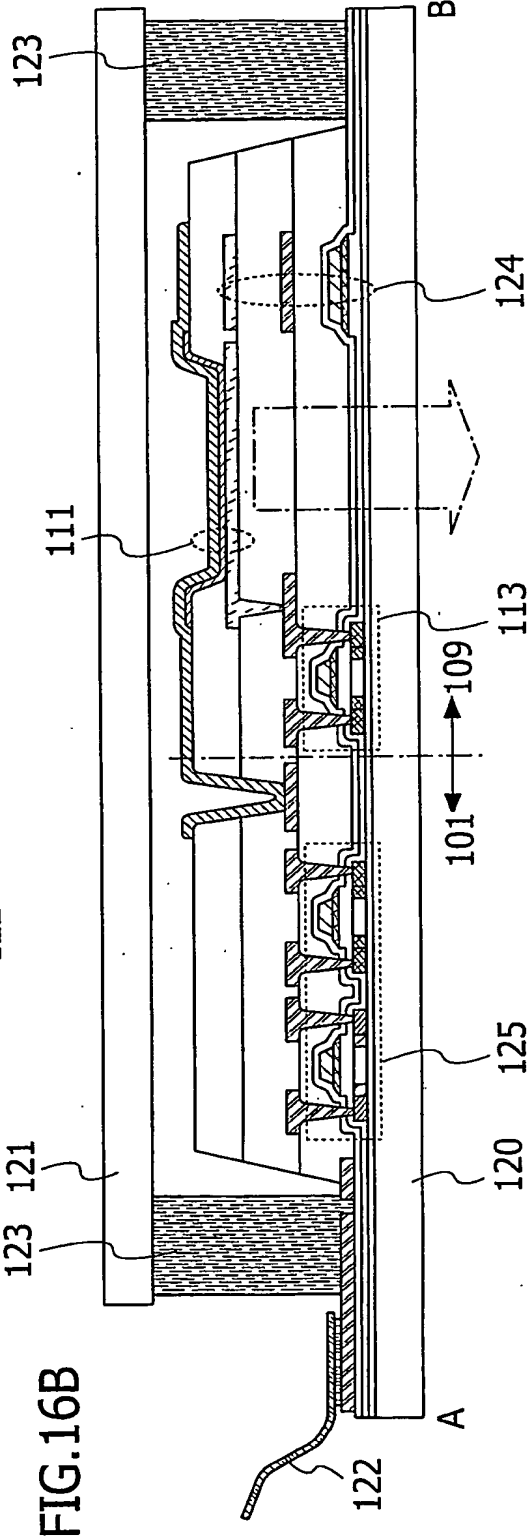
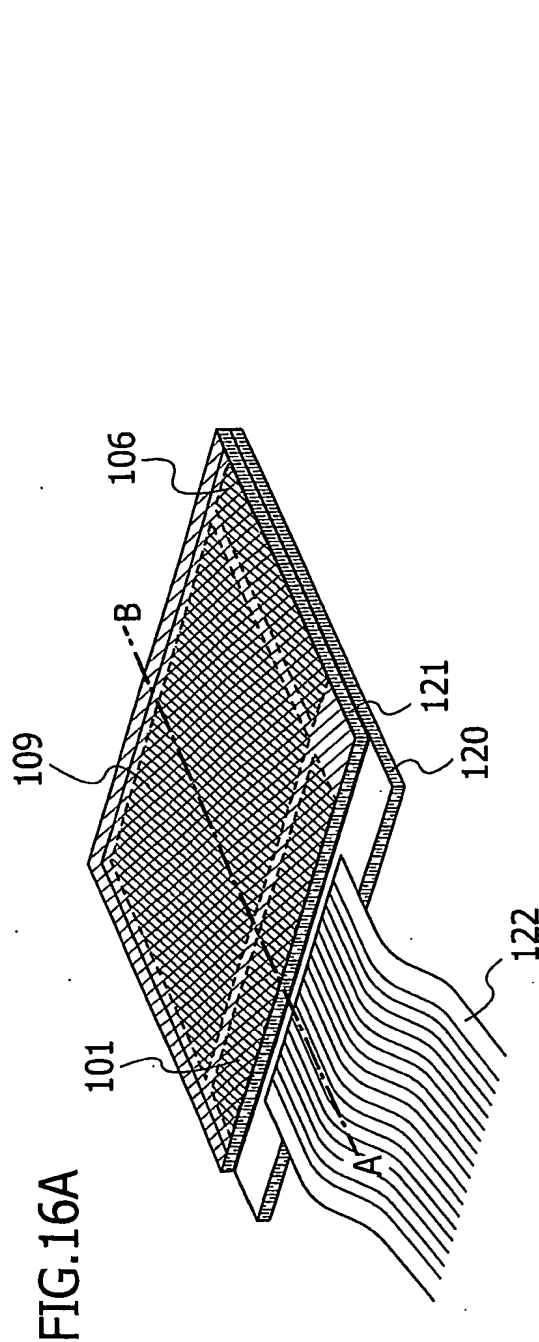
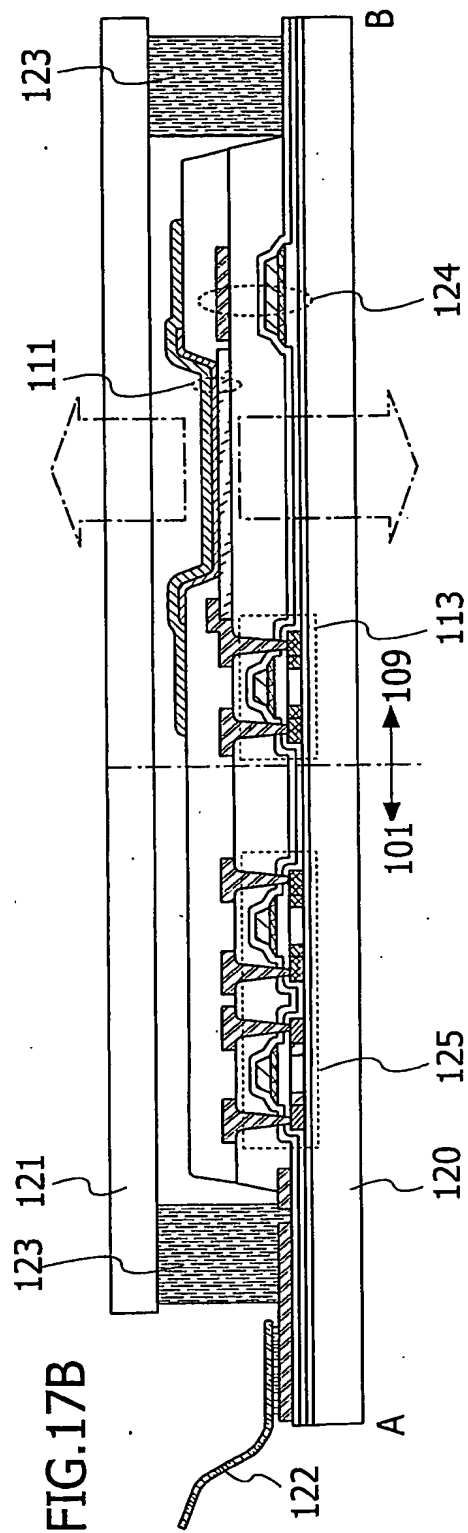
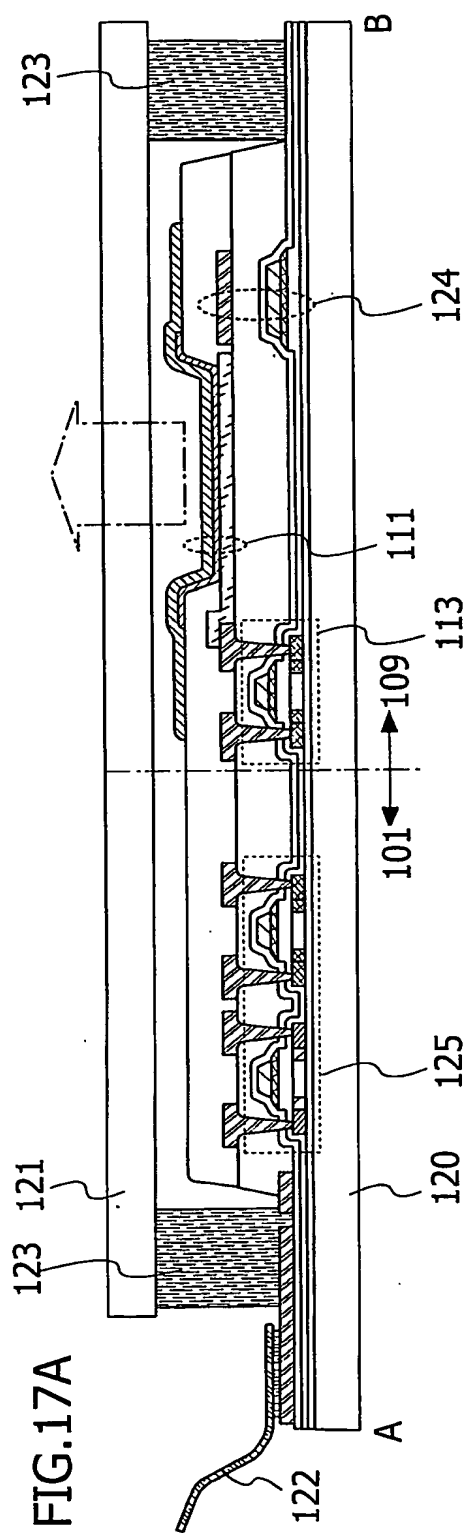


FIG.15



17/25



18/25

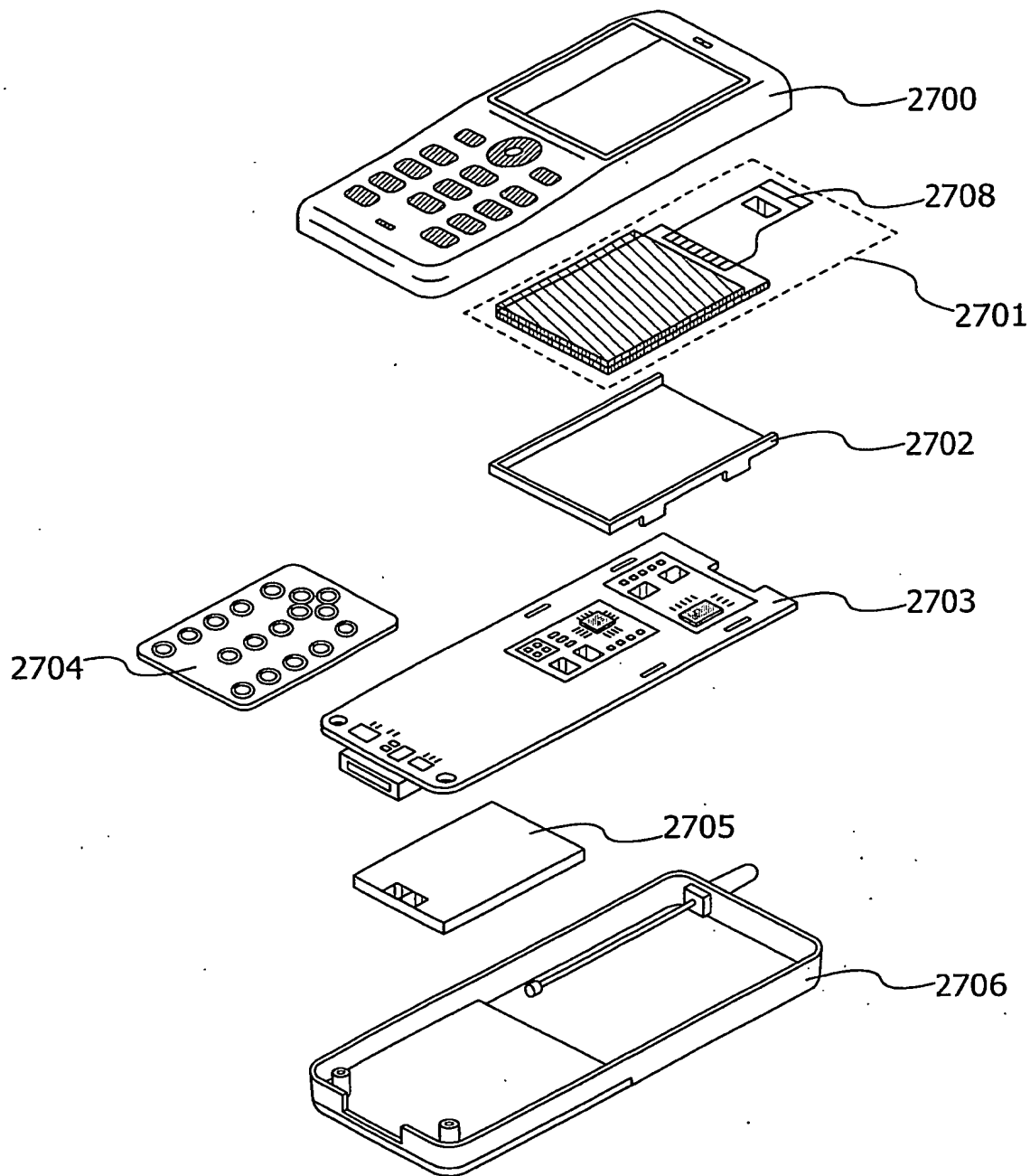
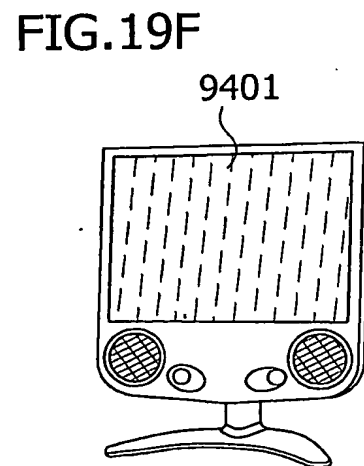
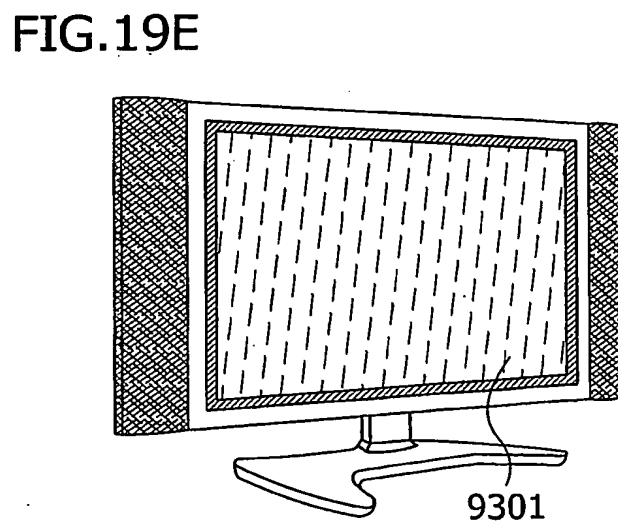
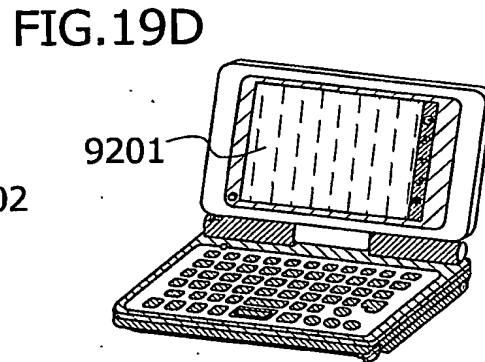
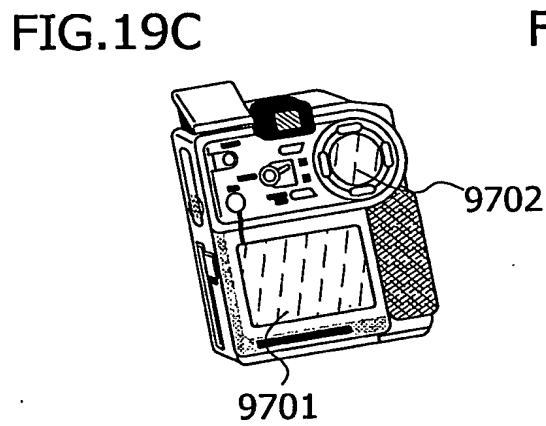
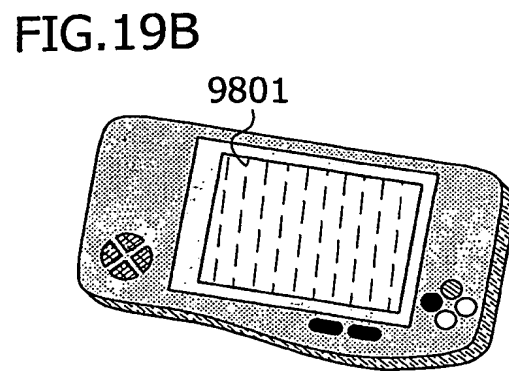


FIG.18

19/25



20/25

FIG.20A

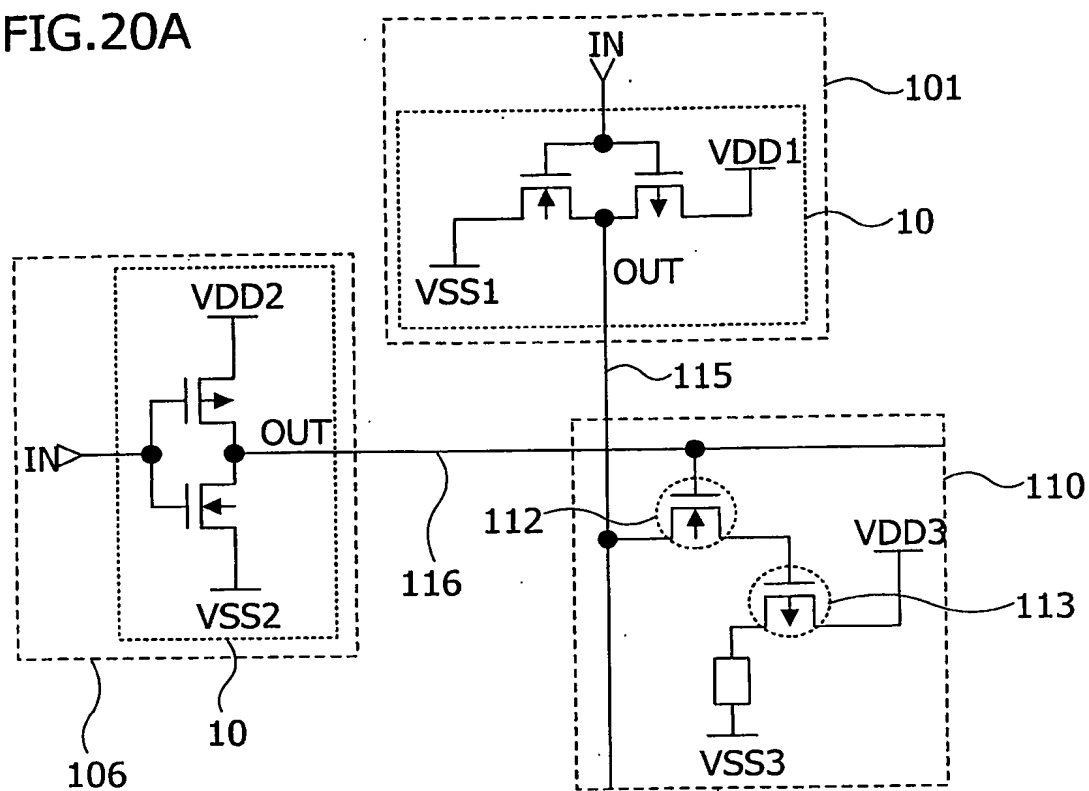


FIG.20B



21/25

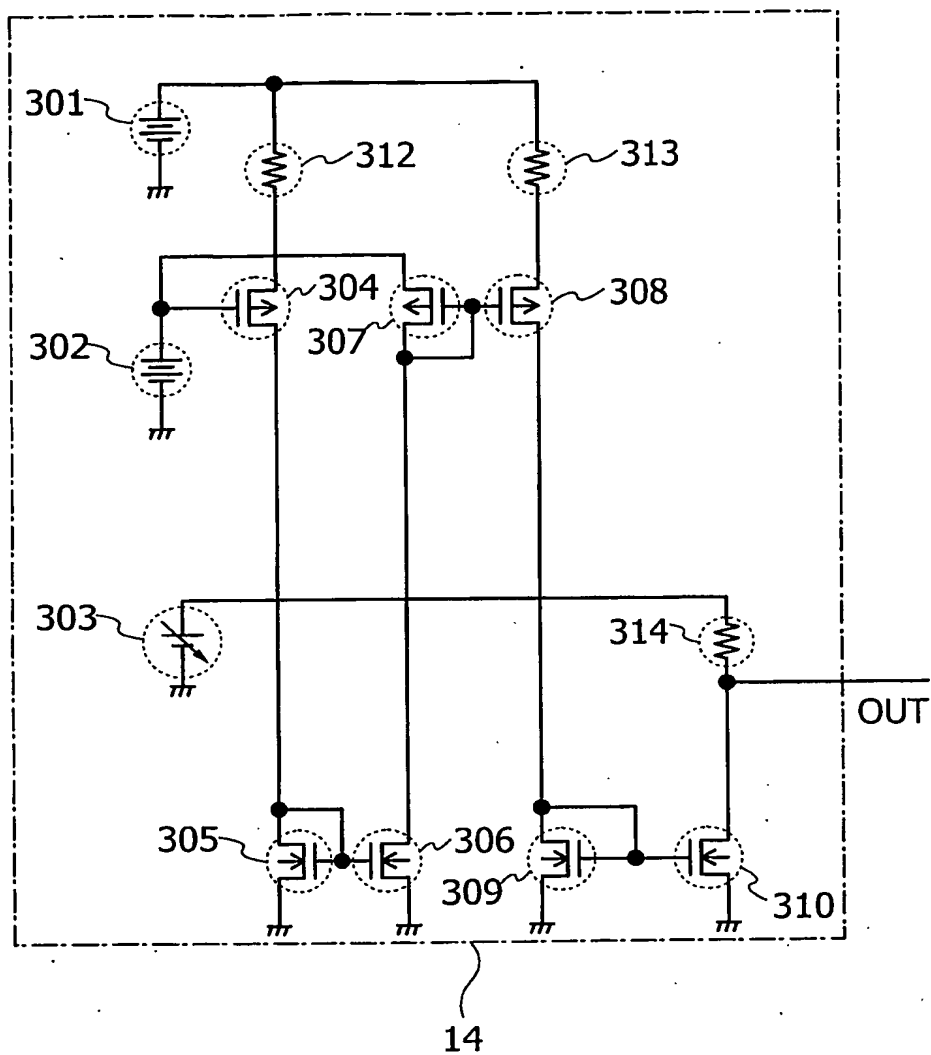
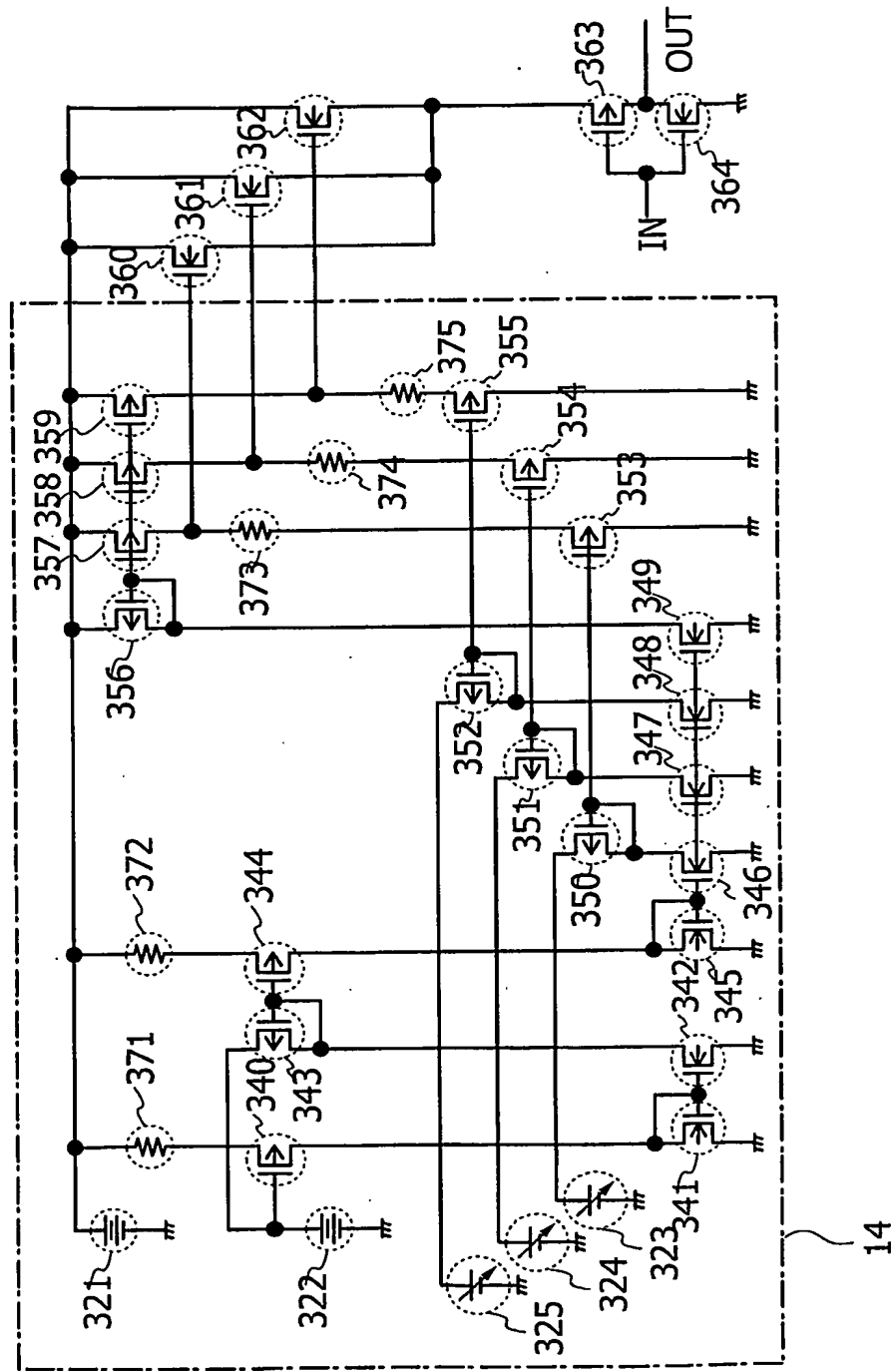


FIG.21

22/25

FIG.22



23/25

FIG. 23A

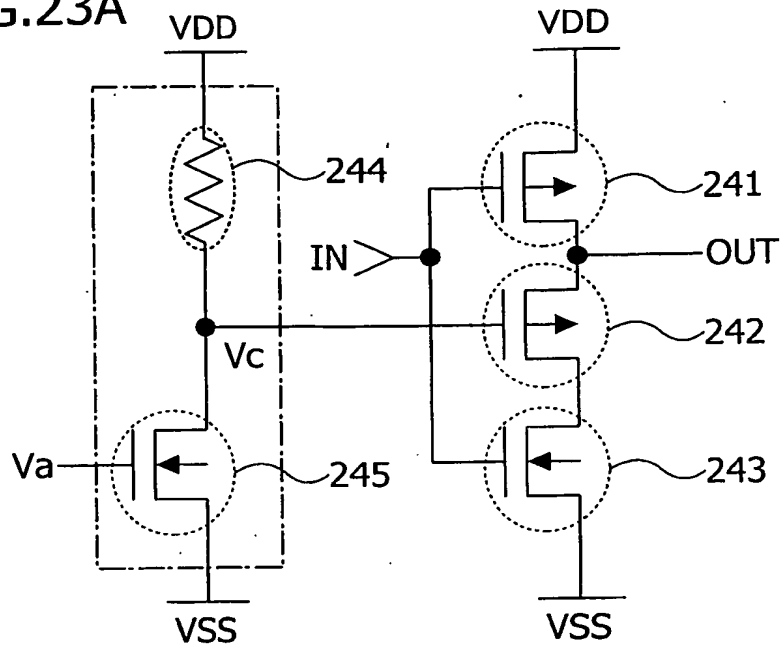
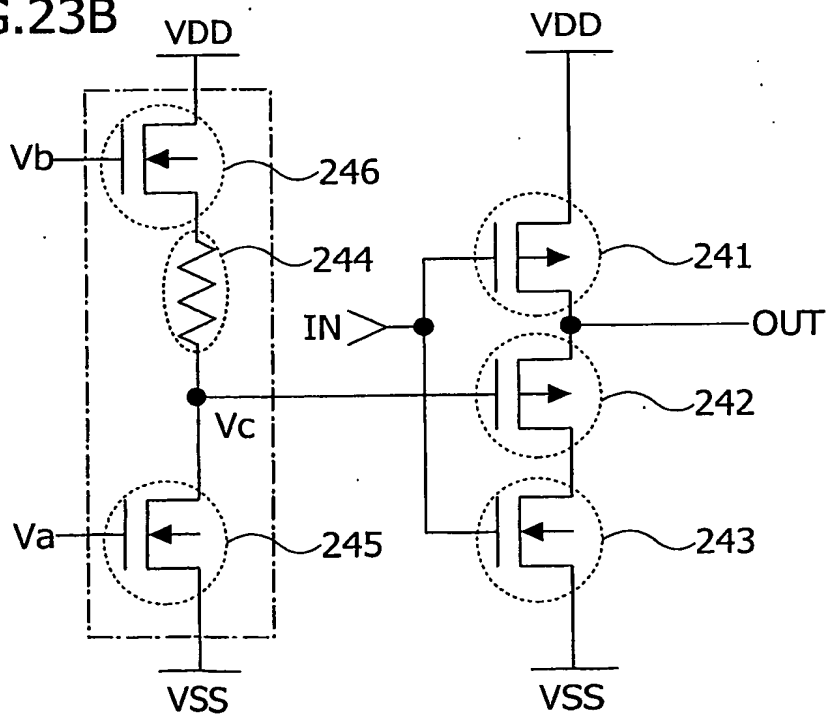


FIG. 23B



EXPLANATION OF REFERENCE

10: signal output circuit, 11: transistor, 12: transistor, 13: transistor, 14: potential
generating circuit, 14a: potential generating circuit, 14b: potential generating circuit, 15:
5 transistor, 21: transistor, 22: transistor, 23: transistor, 24: transistor, 25: transistor, 26:
transistor, 31: transistor, 32: transistor, 33: transistor, 34: transistor, 35: subtraction
circuit, 36: transistor, 37: transistor, 38: subtraction circuit; 51: switch, 52: switch, 53:
capacitor, 54: capacitor, 55: circuit, 56: resistor, 57: resistor, 61: inverter, 101: source
driver, 102: pulse output circuit, 103: latch circuit, 104: latch circuit, 105: buffer circuit,
10 106: gate driver, 107: pulse output circuit, 108: buffer circuit, 109: pixel portion, 110:
pixel, 111: light-emitting element, 112: n-channel transistor, 113: p-channel transistor,
120: substrate, 121: counter substrate, 122: connecting film, 123: sealant, 124: capacitor,
125: multiple elements, 152: monitoring unit, 153: buffer amplifier, 154: constant current
source, 157: monitoring light-emitting element, 158: limiter transistor, 201: transistor,
15 202: transistor, 203: transistor, 204: transistor, 205: transistor, 206: transistor, 207:
transistor, 208: transistor, 209: transistor, 210: transistor, 211: transistor, 212: transistor,
213: transistor, 214: transistor, 215: transistor, 216: transistor, 217: transistor, 218:
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225: transistor, 226: transistor, 227: transistor, 228: transistor, 229: transistor, 230:
20 transistor, 231: transistor, 232: transistor, 233: transistor, 234: transistor, 241: transistor,
242: transistor, 243: transistor, 244: resistor, 245: transistor, 246: transistor, 301: power
source, 302: power source, 303: power source, 304: transistor, 305: transistor, 306:
transistor, 307: transistor, 308: transistor, 309: transistor, 310: transistor, 312: resistor,
313: resistor, 314: resistor, 321: power source, 322: power source, 323: power source,
25 324: power source, 325: power source, 340: transistor, 341: transistor, 342: transistor,
343: transistor, 344: transistor, 345: transistor, 346: transistor, 347: transistor, 348:
transistor, 349: transistor, 350: transistor, 351: transistor, 352: transistor, 353: transistor,
354: transistor, 355: transistor, 356: transistor, 357: transistor, 358: transistor, 359:
transistor, 360: transistor, 361: transistor, 362: transistor, 363: transistor, 364: transistor,
30 371: resistor, 372: resistor, 373: resistor, 374: resistor, 375: resistor, 2700: housing,

2701: panel, 2702: housing, 2703: printed wiring board, 2704: operating button, 2705: battery, 2706: housing, 2708: connecting film, 9102: pixel portion, 9201: pixel portion, 9301: pixel portion, 9401: pixel portion, 9701: pixel portion, 9702: pixel portion, 9801: pixel portion

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2005/022901

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H03K19/0175 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H03K19/0175 (2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
 Published unexamined utility model applications of Japan 1971-2006
 Registered utility model specifications of Japan 1996-2006
 Published registered utility model applications of Japan 1994-2006

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 8-107345 A (FUJITSU LIMITED), 1996.04.23, Figs. 1, 2, 4 (Family : none)	1-4, 21
X	JP 11-163715 A (SIEMENS AKTIENGESELLSCHAFT), 1999.06.18, Fig. 6 & US 5939937 A & EP 905902 A2 & CN 1221256 A & TW 388981 B	5, 6, 21
X	JP 2000-40366 A (Hitachi, Ltd.), 2000.02.08, Figs. 9, 11, 15, 34 & JP 3102428 B	5-12, 19-21
X	JP 2004-159197 A (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.), 2004.06.03, Fig. 1 (Family : none)	5, 6, 19-21

☒ Further documents are listed in the continuation of Box C.☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

09.02.2006

Date of mailing of the international search report

21.02.2006

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Authorized officer

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8 5 2 3

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2005/022901

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 58-64828 A (KABUSHIKI KAISHA TOSHIBA), 1983.04.18, Figs. 4, 5 (Family : none)	13-18, 21
X	JP 58-162130 A (Oki Electric Industry Co., Ltd.), 1983.09.26, Fig. 2 (Family : none)	13-18, 21
X	JP 62-125713 A (KABUSHIKI KAISHA TOSHIBA), 1987.06.08, Fig. 2 (Family : none)	13-18, 21
X	JP 4-236516 A (SONY CORPORATION), 1992.08.25, Fig. 1 & US 5276365 A & KR 225549 B	13-18, 21